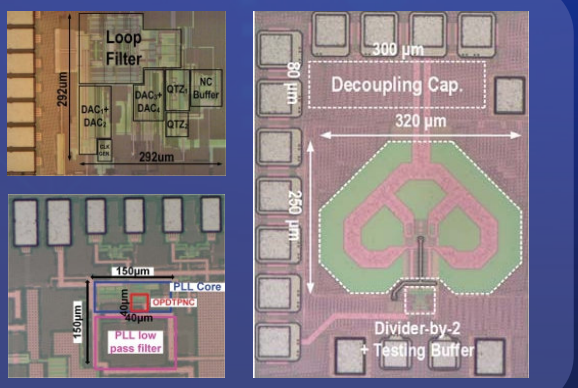
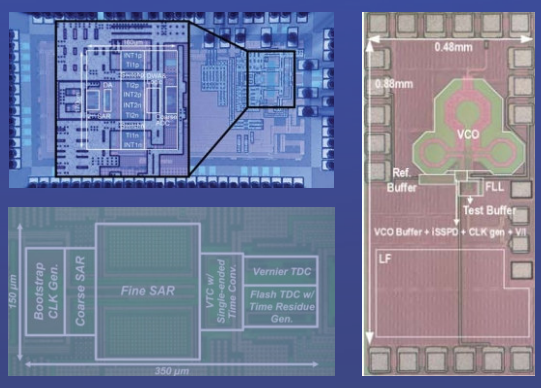
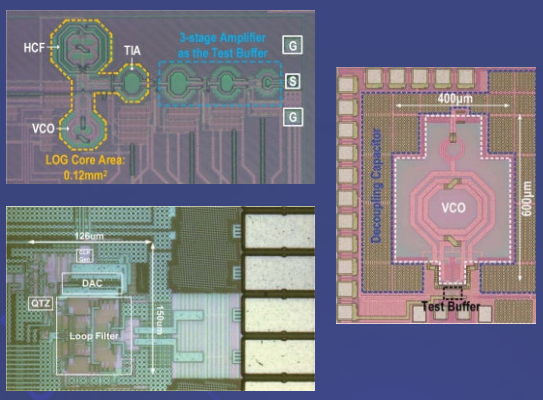
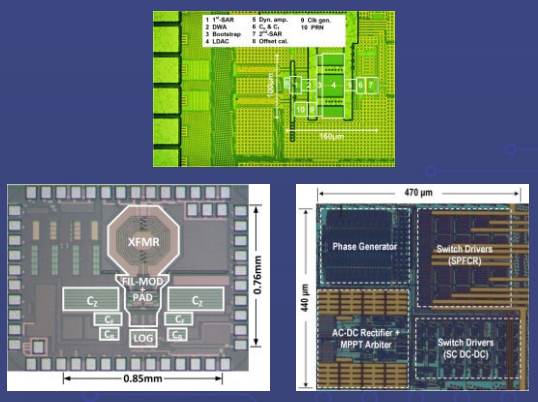
Research Report 2017-2020

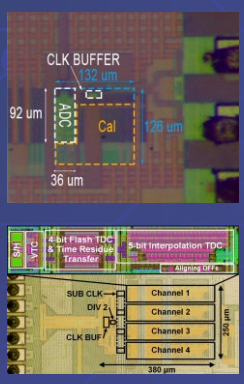
State Key Laboratory of Analog and Mixed-Signal VLSI
University of Macau

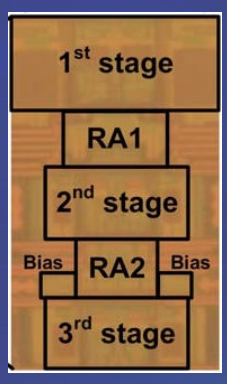


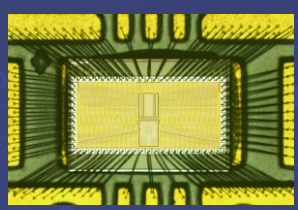


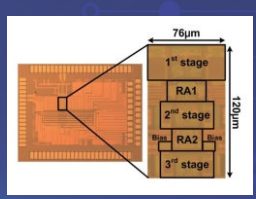


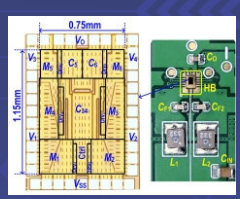












CONTENTS

ACKNOWLEDGEMENTS 01

FOREWORD 03

ORGANIZATIONAL CHART 04

ACADEMIC COMMITTEE 05

RESEARCH ABSTRACTS 07

Wireless Transceivers 07
Wireline Integrated Circuits 24
High Resolution ADCs 33
High Speed ADCs 40
Sub-GHz to GHz ADCs 46
Analog and Mixed-Signal Circuits 53
Biomedical Electronic Devices 58
Energy Harvesting and Sensing Circuits 72
Lab-on-a-Chip 79
Power Management and Conditioning Circuits 87

LIST OF PATENTS 105

SPIN-OFF COMPANY 107

OUR TEAM 108

FACULTY PROFILES 109

RESEARCH INNOVATION CENTERS 128

THESES AWARDED 132

PROJECTS 135

EXPERIMENTAL PROTOTYPES 137

TESTING EQUIPMENT AND FACILITIES 147

ACKNOWLEDGEMENTS

Laboratory Support

Mingzhong Li, Post-Doctoral Fellow for Technical Support
Weng-Ian Chong, Laboratory Assistant
Peishan Li, Laboratory Assistant
Ian-Kei Pun, Laboratory Assistant

Industrial Collaboration

Allwinner
Amicro
AMS
Anyka
Belling
Cadence
Empyrean
Giantech
Global Foundries
IMEC
Keysight
Mentor Graphics
Microtera
National Instruments
Rhode & Schwarz
SMIC
STMicroelectronics
Synopsys
Sytrons
TSMC
UMC
UMEC
XFAB

Sponsored by

Ministry of Science and Technology, China
Macau Science and Technology Development Fund (FDCT)
University of Macau
University of Macau Development Fund
Macau Higher Education Fund

With the collaboration of

IEEE Macau Section
IEEE Macau Section SSCS Chapter
IEEE Macau Section CAS/COM Joint Chapter

FOREWORD

Inaugurated in January 25, 2011, the State Key Laboratory of Analog and Mixed-Signal VLSI **(SKL-AMSV)** at University of Macau (UM) completed this year the first decade of its existence. After the first phase of development (2011-2013) when the *main human and technical infrastructures of the laboratory were set-up* and positively assessed by the MoST after 3 years, we entered a second phase of evolution (2014-2016) where we assisted to the *consolidation and further integration of the different research lines*, already in a new world-class facility in the new UM campus, in Hengqin. In 2017, after the second positive evaluation by the MoST we initiated a new period (2017-2019) where we *maintained our world-level state-of-the-art electronics status while we expanded our commercialization activity*. This, was possible through the set-up of a second branch of the SKL-AMSV in the Microelectronics Center of the Zhuhai UM Research Institute that gradually started the collaboration with the top Chinese companies in electronics by setting in motion several commercial projects. Besides this, we also launched in Hengqin the first spin-off company of UM, designated by Digifluidics, where the CEO is a PhD graduate from the lab. Our dimensions, in terms of human and space resources are still of a medium scale, but the work developed is of extremely high quality, with world-top level results, and we've the ambition to contribute further, with great determination and hard work, for the development of state-of-the-art electronics in China. Subsequently, in our plan for the 4th period of development (2020-2022) we proposed *to advance further the state-of-the-art electronics and microsystems for emerging applications and commercialization*, in order to be in line with our original **Motto: Locally, from (World) Quality towards (National) Quantity**, created in 2011 but that is always present in our minds and reflects well our constant development. Important façades of the SKL-AMSV rigorously documented throughout the years by the papers (chips) published there, are the *IEEE ISSCC* and the *IEEE JSSC*. In the period 2017-2020 with 30 papers in *ISSCC*, we maintained the leadership in China, Hong Kong and Macao, and were consistently yearly in the Top 10 in the World, placed in 2019, with 8 papers (chips) only behind Intel. In addition, between 2018 and 2020 with 29 papers (chips) in *JSSC* we were in 9th place in the World, in a table led by INTEL with 49. Besides, in the period covered by this report (2017-2020) our overall results included: 7 books and chapters; 196 international refereed journal articles (36 in *JSSC*); 110 international conference papers (30 in *ISSCC*); 19 US patents; 8 China Patents; 31 PhD graduates; 37 MSc graduates; 3 Technological Invention Awards from the Macao Science and Technology Development Fund (FDCT), with 1st and 2nd prizes in 2020; 3 FDCT Postgraduate awards (PhD) and 1 *Takuo Sugano Award* for Outstanding Far-East Paper (ISSCC 2018) (first attributed to a team from China).

We will continue striving always for the best at the SKL-AMSV!

Prof. Rui Martins
Director, SKL-AMSV
UM, October 5, 2021

ORGANIZATIONAL CHART

Academic Team 學術團隊

Management 管理

Prof. Rui MARTINS
馬許願教授
IEEE Fellow IEEE會士
Director of SKL - AMSV
國家重點實驗室主任
Director of IME
研究院院長

Prof. Pui In MAK
麥沛然教授
IEEE Fellow IEEE會士
Deputy Director of SKL-AMSV
國家重點實驗室副主任
Deputy Director (Research) of IME
研究院副院長（研究）

Prof. Sai Weng SIN
冼世榮副教授
Associate Director (Academic) of SKL-AMSV
國家重點實驗室副主任（學術）
Deputy Director (Academic) of IME
研究院副院長（學術）

Prof. Franco MALOBERTI
Chair of SKL Academic Committee
(Scientific Advisory Board)
實驗室學術委員會主席

Prof. Man Kay LAW
羅文基副教授
Laboratory Infrastructure Coordinator
實驗室基礎設施協調主任

Prof. Yan ZHU
諸嫣副教授
Industrial Collaboration Coordinator
產業合作協調主任

Prof. Yan LU
路延副教授
Microelectronics Center / ZUMRI Coordinator
珠海澳大科技微電子研發中心主任

Wireless and Multidisciplinary Innovation Center(WMIC) 無線和多學科創新中心

Pui In MAK
麥沛然
Full Professor
教授

Man Kay LAW
羅文基
Associate Professor
副教授

Sio Hang PUN
潘少恆
Associate Professor
副教授

Jun YIN
殷俊
Associate Professor
副教授

Yong CHEN
陳勇
Assistant Professor
助理教授

Yanwei JIA
賈艷偉
Assistant Professor
助理教授

Ka Fai UN
阮家燁
Assistant Professor
助理教授

Ka Meng LEI
李家明
Assistant Professor
助理教授

Yang JIANG
江洋
Assistant Professor
助理教授

Wei Han YU
于維翰
Assistant Professor
助理教授

Data and Power Conversion Innovation Center(DPIC) 數據和電源轉換創新中心

Sai Weng SIN
冼世榮
Associate Professor
副教授

Yan ZHU
諸嫣
Associate Professor
副教授

Chi Seng LAM
林智聲
Associate Professor
副教授

Yan LU
路延
Associate Professor
副教授

Chi Hang CHAN
陳知行
Assistant Professor
助理教授

Mo HUANG
黃沫
Assistant Professor
助理教授

Minglei ZHANG
張明磊
Assistant Professor
助理教授

Administrative and Technical Team 行政技術團隊

Fan NG, Leo
吳凡
Functional Head (Operation)
事務主管（運行）

Un Pang LEI, Lewis
李遠鵬
Functional Head (Technical)
事務主管（技術）

Bin ZHOU, Jet
周 斌
Technology Transfer Officer
技術轉移主任

Chi Wai TANG, Kevin
鄧志偉
Laboratory Technician - Safety Officer
實驗室技術員 — 安全主任

Yuen Ki CHAN, Elizabeth
陳婉琪
Administrative Officer
行政主任

Jie GAO, Jennie
高潔
Laboratory Technician
實驗室技術員

Jianyu ZHONG, Jankey
鍾健瑜
Laboratory Technician
實驗室技術員

Pui Wan SOU, Jenny
蘇佩雲
Senior Administrative Assistant
高級行政助理

Sut Wai IEONG, Hedy
楊雪慧
Administrative Assistant
行政助理

ACADEMIC COMMITTEE

SKL Academic Committee (12 IEEE Fellows)
國家重點實驗室學術委員會（12名IEEE會士）

2012-2023

Prof. Franco MALOBERTI
IEEE Fellow
University of Pavia

Prof. Zhiliang HONG
Fudan University

Prof. Howard Cam LUONG
IEEE Fellow
Hong Kong University of Science and Technology

Prof. Akira MATSUZAWA
IEEE Fellow
Tokyo Institute of Technology

Prof. Bram NAUTA
IEEE Fellow
University of Twente * 1

Prof. Behzad RAZAVI
IEEE Fellow
University of California, Los Angeles * 2

Prof. Zhihua WANG
IEEE Fellow
Tsinghua University

Prof. Hoi-Jun YOO
IEEE Fellow
Korea Advanced Institute of Science and Technology

2018-2023

Prof. Baher HAROUN
IEEE Fellow
Texas Instruments

Prof. Ming LIU
IEEE Fellow
IME of Chinese Academy of Sciences * 3

Prof. Boris MURMANN
IEEE Fellow
Stanford University

Prof. Robert Bogdan STASZEWSKI
IEEE Fellow
University College Dublin

Prof. Peter Chung-Yu WU
IEEE Fellow
Yang Ming Chiao Tung University

13 eminent IC experts(12 IEEE Fellows) 13名傑出的IC專家（12名IEEE會士）

3 Academicians(China,US and The Netherlands) 3名院士（中國,美國和荷蘭）

* 1:Member of the Royal Netherlands Academy of Arts and Sciences 荷蘭皇家藝術與科學學院院士
* 2:Member of the United States National Academy of Engineering 美國國家工程院院士
* 3:Member of the Chinese Academy of Sciences 中國科學院院士

Wireless Transceivers

A 0.2V energy-harvesting BLE transmitter with a micropower manager achieving 25% system efficiency at 0dBm output and 5.2 nW sleep power in 28nm CMOS -------- 08

A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS -------- 09

A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) P_{out} -------- 10

A 0.0056-mm² -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs -------- 11

A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA -------- 12

A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push-Pull LNA -------- 13

An Inverse-Class-F CMOS Oscillator with Intrinsic- High-Q 1st -Harmonic and 2nd -Harmonic Resonances -------- 14

Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools -------- 15

A 0.7-to-2.5 GHz, 61% EIRP System Efficiency, 4-Element MIMO TX Exploiting Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver -------- 16

A 0.12-mm² 1.2-to-2.4 mW 1.3-to-2.65 GHz Fractional-N Bang-Bang Digital PLL with 8-µs Settling Time for Multi-ISM-Band ULP Radios -------- 17

Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection -------- 18

A 0.038mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop -------- 19

A Multiband FDD SAW-less Transmitter for 5G-NR Featuring a BW-Extended – Path Filter-Modulator, a Switched-BB Input and a Wideband TIA-Based PA Driver -------- 20

A SAW-less Tunable RF Front-End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA -------- 21

A 0.096-mm² 1–20-GHz Triple-Path Noise Canceling Common-Gate Common-Source LNA With Dual Complementary pMOS–nMOS Configuration -------- 22

Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled MM-Wave VCO Using a Single-Center-Tapped Switched Inductor -------- 23

A 0.2V energy-harvesting BLE transmitter with a micropower manager achieving 25% system efficiency at 0dBm output and 5.2 nW sleep power in 28nm CMOS

J. Yin, S. Yang, H. Yi, W.-H. Yu, P.-I. Mak and R. P. Martins

FEATURES

Low supply voltage for energy harvesting, 0.2 V
High power efficiency BLE TX, 25% @ 0 dBm
Low leakage power, 5.2 nW
Low spur PLL
HD suppressed PA
Silicon verified in TSMC 28nm CMOS

DESCRIPTION

This paper reports an ultralow-voltage (ULV) energy-harvesting bluetooth low-energy (BLE) transmitter (TX). It features: 1) a fully integrated micropower manager (µPM) to customize the internal supply and bias voltages for both active and sleep modes; 2) a gate-to-source- coupling ULV voltage-controlled oscillator (VCO) using a high-ratio (5.6:1) stacking transformer to improve the phase noise and output swing; 3) an ULV class-E/F2 power amplifier (PA) with an inside-transformer LC notch to suppress the HD3, and finally 4) an analog type-I phase-locked loop (PLL) with a reduced duty cycle of its master-slave sampling filter (MSSF) to suppress the jitter and reference spur. The TX prototyped in 28-nm CMOS occupies an active area of 0.53 mm² and exhibits 25% system efficiency at 0-dBm output at a single 0.2-V supply. Without resorting from any external components, both the output HD2 (−49.6 dBm) and HD3 (−47.4 dBm) comply with the BLE standard. The FSK error is 2.84% and the frequency drift in a 425-µs data packet is <5 kHz under open-loop modulation. The use of negative-voltage power gating suppresses the sleep power of the entire TX to 5.2 nW.

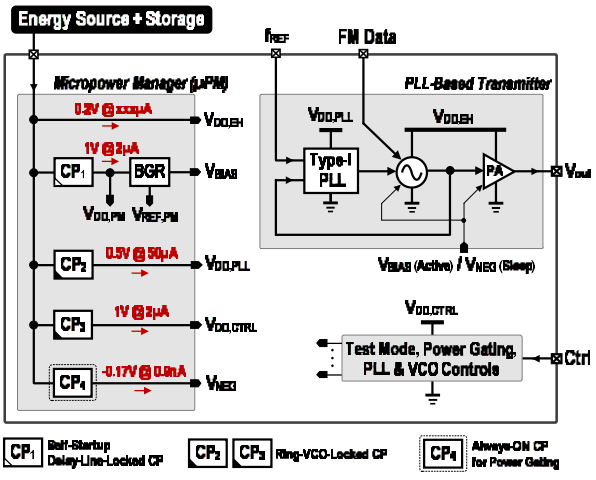


Fig. 1. Proposed energy-harvesting BLE TX with a fully integrated µPM to generate the internal supply and bias voltages that are insensitive to the voltage variation of the energy-harvester output (VDD,EH) down to 0.2 V.

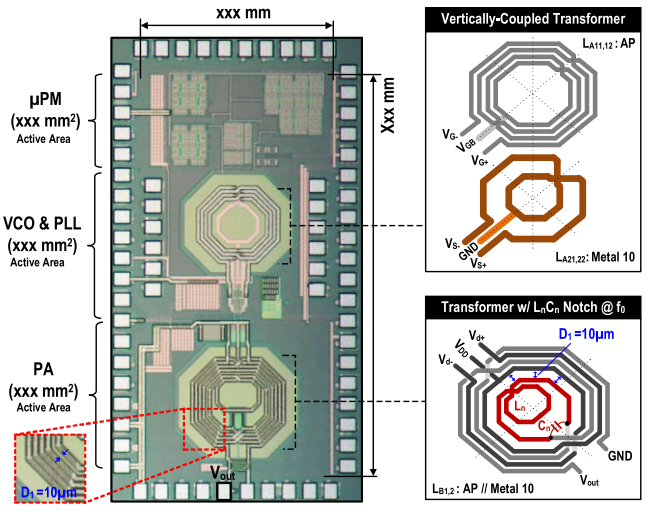


Fig. 2. Chip micrograph.

Publication(s)

[1] Jun Yin, Siheng Yang, Haidong Yi, Wei-Han Yu, Pui-In Mak, Rui Martins, “A 0.2V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0dBm Output and 5.2nW Sleep Power in 28nm CMOS,” IEEE International Solid-State Circuits Conference (ISSCC), Digest., pp. 450-451, Feb. 2018.

[2] Shiheng Yang, Jun Yin, Haidong Yi, Wei-Han Yu, Pui-In Mak, and Rui P. Martins, “A 0.2-V Energy-Harvesting BLE Transmitter With a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS,” IEEE Journal of Solid-State Circuits, vol.54, pp. 1351-1362, May. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS

Wei-Han Yu, Haidong Yi, Pui-In Mak, Jun Yin, R. P. Martins

FEATURES

Low supply voltage for energy harvesting, 0.18 V
Ultra-low power BLE RX, 382 µW
Low leakage power, 1.3 nW
Fast start-up µPM
Power-gating LNA
Silicon verified in TSMC 28nm CMOS

DESCRIPTION

We propose an ultra-low-voltage Bluetooth low-energy (BLE) receiver (RX) front end with an on-chip micropower manager (µPM) to customize the internal voltage domains. It aims at direct powering by the sub-0.5-V energy harvesting sources like the on-body thermoelectric, eliminating the loss and cost of the interim dc–dc converters. Specifically, the RX incorporates: 1) a two-stage power-gating low-noise amplifier with fully on-chip input-impedance matching and passive gain boosting reducing both the active and sleep power; 2) a class-D voltage-controlled oscillator (VCO) in parallel with a class-C starter to secure a fast startup; and 3) a µPM using ring VCO-locked charge pumps and bandgap references to withstand the supply-voltage variation (0.18–0.3 V). Fabricated in 28-nm CMOS, the RX operates down to a 0.18-V supply, while exhibiting 11.3-dB NF and −12.5-dBm out-of-band IIP3. The VCO shows < −113 dBc/Hz phase noise at 2.5-MHz offset. The active and sleep power are 382 µW and 1.33 nW, respectively.

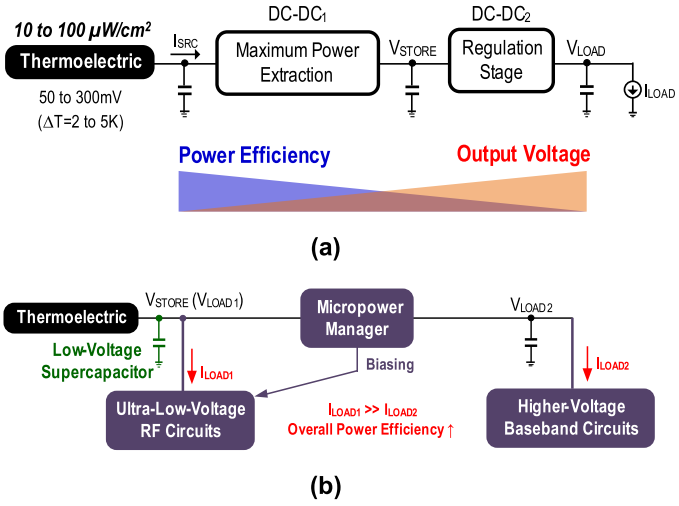


Fig. 1. (a) Conventional energy-harvesting topology. and (b) Codesign between our proposed energy-harvesting topology and ULV RF circuits, where a µPMcan provide the critical biases and support the standard voltage BB circuits.

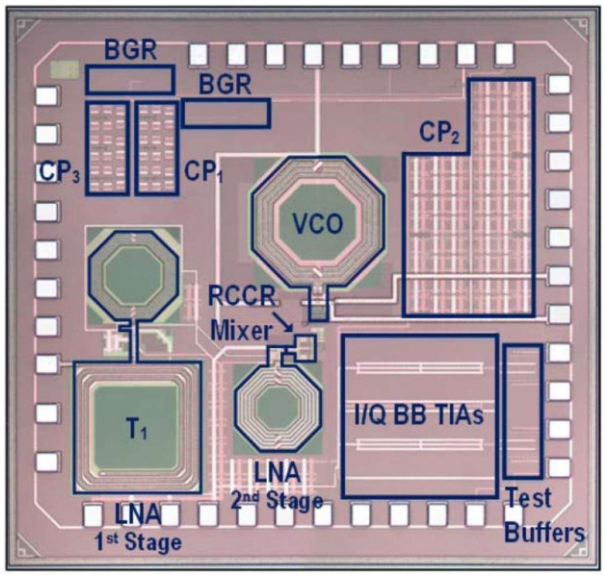


Fig. 2. Chip micrograph.

Publication(s)

[1] Wei-Han Yu, Haidong Yi, Pui-In Mak, Jun Yin, R. P. Martins, “A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS,” IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 414-415, Feb. 2017.

[2] Haidong Yi, Wei-Han Yu, Pui-In Mak, Jun Yin and R. P. Martins, “A 0.18-V 382-µW Bluetooth Low-Energy (BLE) Receiver with 1.33-nW Sleep Power for Energy-Harvesting Applications in 28-nm CMOS,” IEEE Journal of Solid-State Circuits, vol. 53, pp. 1618-1627, Aug. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) P_{out}

Xingqiang Peng, Jun Yin, Pui-In Mak, Wei-Han Yu and R. P. Martins

FEATURES

Function-Reuse Class DCO-PA
High power efficiency ZigBee TX, 22.6% @ 6 dBm
Scalable supply voltage, 0.3-0.7 V
Low distortion, 2.29% EVM.
Compact area, 0.39 mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper describes a sub-1-V 2.4-GHz ZigBee transmitter (TX) with scalable output power (P_{out}) and system efficiency. It features a function-reuse class-F topology unifying the digital-controlled oscillator (DCO) and power amplifier (PA), designated as DCO-PA. Unlike the existing current reuse topologies that rely on transistor stacking, here the power consumption of the DCO and PA-driver is absorbed into the DCO-PA without losing the voltage headroom, while allowing a low supply voltage. The DCO-PA also benefits from a six-port transformer with customized coupling coefficients and turn ratios to jointly perform the functions of resonant tank and output matching network, saving the chip area. A fractional-N all-digital phase-locked loop (ADPLL) realizes a two-point data modulation. Its phase-interpolated time-to-digital converter prevents time-consuming calibration. The entire TX fabricated in 65-nm CMOS occupies a 0.39-mm² active area. The standalone DCO-PA shows a peak efficiency of 26.2% at a 6-dBm P_{out}, and a back-off efficiency of 17.7% at a −4.3 dBm P_{out} under a scalable supply voltage (0.3–0.7 V). The system efficiency, including the ADPLL, is 22.6% (14.5%) at 6-dBm (0-dBm) P_{out}. The HS-OQPSK modulated output complies with the ZigBee spectral mask with an adequate margin and the error vector magnitude is 2.29%.

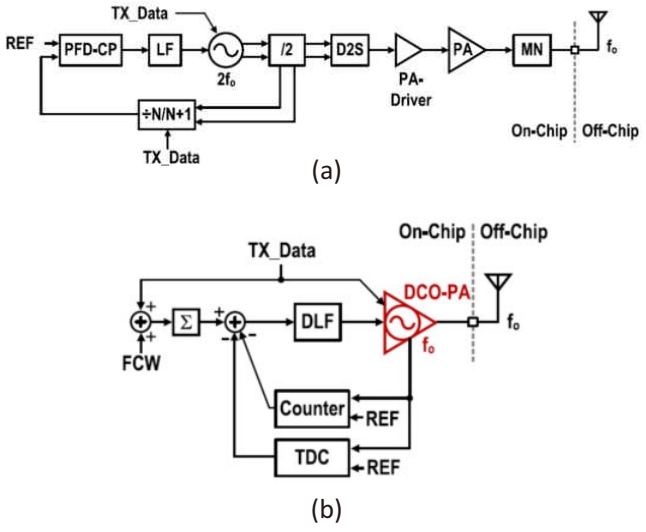


Fig. 1. ULP TXs using (a) conventional separated VCO and PA, and (b) proposed function re-use DCO-PA.

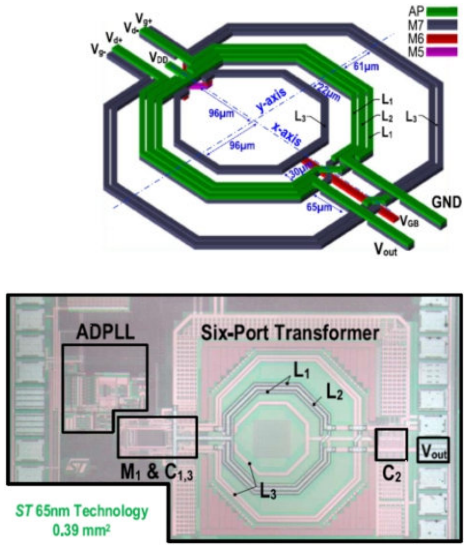


Fig. 2. Chip micrograph.

Publication(s)

[1] Xingqiang Peng, Jun Yin, Pui-In Mak, Wei-Han Yu and R. P. Martins, "A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) P_{out}," IEEE Journal of Solid-State Circuits, vol. 52, pp. 1495- 1508, Jun. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.0056-mm² -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs

Shiheng Yang, Jun Yin, Pui-In Mak, and Rui P. Martins

FEATURES

A low-power block-sharing offset-free frequency-tracking loop (FTL) to calibrate the PVT variations of the voltage-controlled oscillator (VCO) frequency

Varactor-tuned dual multiplexed-ring VCOs to reduce jitter variation while extending the frequency tuning range.

Silicon verified in GF 28 nm CMOS

A state-of-the-art Jitter-FoM of −249 dBc/Hz at 3 GHz

DESCRIPTION

This work proposes an ultra-compact all-digital multiplying delay-locked loop (MDLL) featuring a low-power block-sharing offset-free FTL to calibrate the PVT variations of the VCO frequency. Such FTL utilizes a digital-controlled delay line (DCDL)-based low-power time-interval comparator and an adjacent-edge selector, to precisely detect the static phase offset (SPO) caused by the VCO frequency drifting in the presence of reference injection. The block-sharing-based SPO detection aids in nullifying the circuit-mismatch- and offset-induced deterministic error. Also, for the adjacent edge selector, block sharing between its control generation circuits and the coarse FTL further reduces the power consumption. The varactor-tuned dual multiplexed-ring VCOs (MRVCOs) serve to reduce jitter variation while extending the frequency tuning range.

Prototyped in a 28-nm CMOS with a core area of 0.0056 mm², the proposed MDLL covers a tuning range from 1.55 to 3.35 GHz, and exhibits a root-mean-square (rms) jitter of 292 fs at the 3-GHz output, under a 200-MHZ reference clock. The power consumption is 1.45 mW at a 0.8-V supply, resulting in an FoM of −249 dB favorably comparable with state-of-the-art.

Benchmarking with the recent ring-VCO-based MDLLs and ILCMs, this work shows improved area efficiency of >4.2× and FoM referring to the reference frequency (FoMr) of >2dB. Moreover, the FTL's power consumption of 0.3mW is the lowest reported.

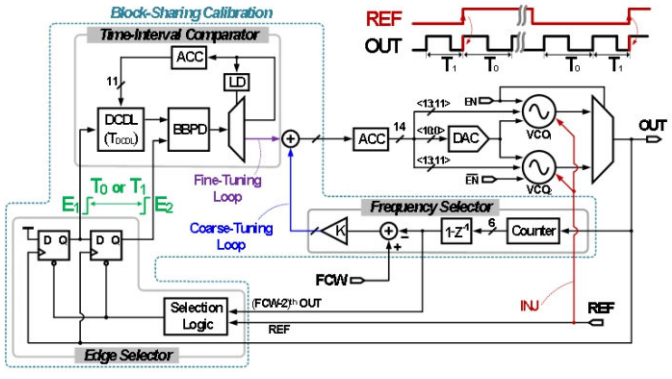
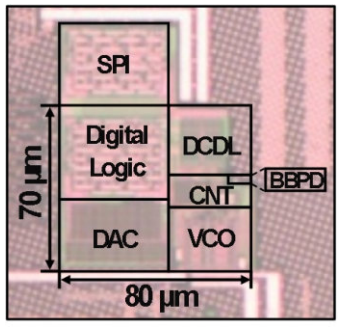


Fig. 1. Proposed all-digital MDLL architecture.



(a)

Power Consumption (mW)	
Digital Logic	0.2
AES and TIC*&	0.04
Counter	0.02
DAC	0.03
VCO	1.16
Total	1.45

* AES: Adjacent Channel Selector, TIC: Time-Interval Comparator.
& Power of comparison logic in AES is included in the digital logic.

(b)

Fig. 2. (a) Chip micrograph and (b) area breakdown.

Publication(s)

[1] S. Yang, J. Yin, P. -I. Mak, and R. P. Martins, "A 0.0056-mm² -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs," IEEE Journal of Solid-State Circuits, pp. 89-98, vol. 54, Jan. 2019.

[2] S. Yang, J. Yin, P. -I. Mak, and R. P. Martins, "A 0.0056mm² All-Digital MDLL Using Edge Re-extraction, Dual Ring-VCOs and a 0.3mW Block-Sharing Frequency-Tracking Loop Achieving 292fs$_{rms}$ Jitter and -249dB FoM," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 118-119, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of the University of Macau.

A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA

Chao Fan, Jun Yin, Chee-Cheow Lim, Pui-In Mak, and Rui P. Martins

FEATURES

A 60GHz current-reuse LO generator (LOG) employing current-mode implicit frequency tripling

Achieve large output swing, low phase noise, and low subharmonic spurs simultaneously

Silicon verified in TSMC 65 nm CMOS

A state-of-the-art peak FoM of 186.7 dBc/Hz

DESCRIPTION

This work proposes a 60GHz current-reuse LOG featuring current-mode implicit frequency tripling. It includes : 1) a current-output VCO to generate a large 3rd-harmonic current with low phase noise; 2) an area-efficient passive harmonic-current filter (HCF) using the S-shape inductors to reject the 1st- and 2nd-harmonic leakage currents at f_{LO} and $2f_{LO}$; and 3) a current-reuse transimpedance amplifier(TIA) stacked atop the VCO and HCF to recover a large output swing with low power.

Prototyped in 65nm CMOS, the proposed LOG exhibits a high FoM of 184.9 to 186.7dBc/Hz at a 1MHz offset over a frequency tuning range from 54.9 to 63.5GHz (14.5%). The measured subharmonic spurs are <−61dBc.

Benchmarking with the prior art, our LOG exhibits a best-in-class FoM@1MHz and low 1st- and 2nd- harmonic spurs. Specifically, comparing with the voltage-mode implicit frequency tripling technique that entails a buffer stage to boost the 3rd-harmonic voltage while suppressing the large fundamental voltage at the class-F VCO output, our design consumes less power and shows improved FoM@1MHz by >5.2dB, and subharmonic spurs by 10dB.

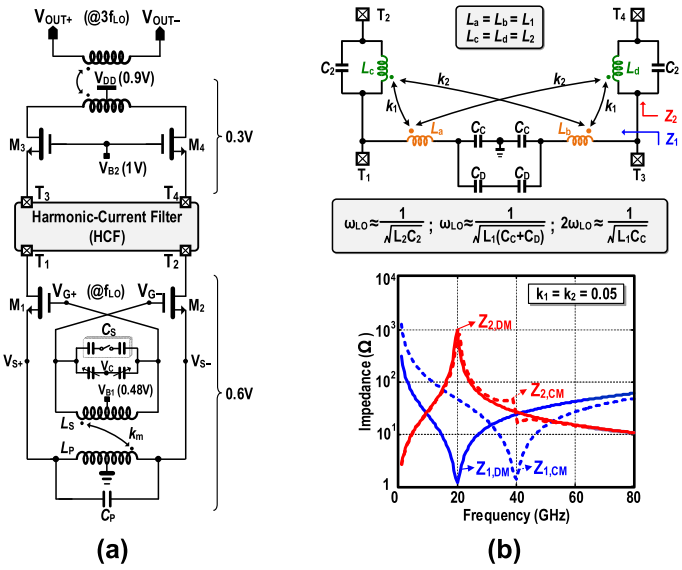


Fig. 1. (a) Proposed 60-GHz LOG using current-mode implicit frequency tripling technique and (b) passive harmonic-current filter.

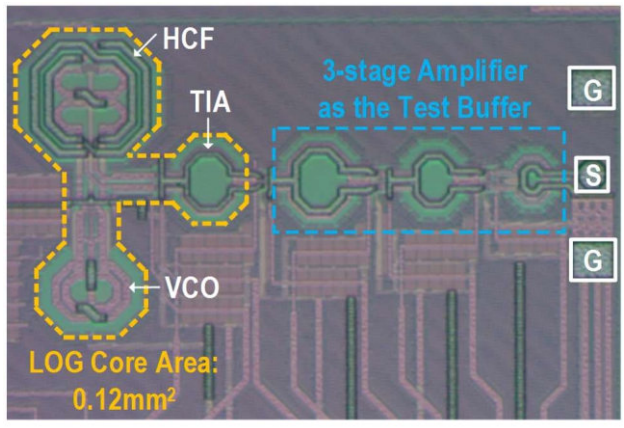


Fig. 2. Chip micrograph.

Publication(s)

[1] C. Fan, J. Yin, C. -C. Lim, P. -I. Mak, and R. P. Martins, "A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 282-283, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push-Pull LNA

Kai Xu, Jun Yin, Pui-In Mak, Robert Bogdan Staszewski, and Rui P. Martins

FEATURES

A function-reuse single-MOS digitally controlled oscillator power amplifier (DCO-PA) improves antenna-to-DCO isolation

A noninverting transmitter matching transformer with a zero-shifting capacitor to suppress the 2nd-harmonic emission of the DCO-PA

A push-pull low-noise amplifier (LNA) reuses the transmitter matching transformer for passive gain boosting

Silicon verified in TSMC 65 nm CMOS

DESCRIPTION

This work proposes a simple power-efficient sub-1-V fully integrated RF front end for 2.4-GHz transceivers. It introduces the following innovations. First, a function-reuse single-MOS DCO-PA with full supply utilization improves antenna-to-DCO isolation for better resilience to jammers. Second, a noninverting transmitter (TX) matching transformer with a zero-shifting capacitor suppresses the second-harmonic emission of the DCO-PA and allows a single-pin antenna interface for both TX and receiver (RX) modes eliminating the transmit/receive (T/R) switches in the signal path. Third, a push-pull low-noise amplifier (LNA) reuses the TX matching transformer for passive gain boosting that reduces power consumption.

Prototyped in 65-nm CMOS, the RF front end occupies merely 0.17 mm². Through the functional merge of the oscillator and PA, it can transmit 0 dBm at RF, featuring 10.2% power efficiency when delivering the RF power as low as −10 dBm at a 0.3-V supply. Under a 0.5-V supply, the LNA shows 11-dB gain and 6.8-dB noise figure while consuming 174 µW.

To the best of our knowledge, the presented single-MOS DCO-PA architecture is the first fully integrated single-ended solution with competitive carrier phase noise and power efficiency, especially at low power modes while simultaneously handling the harmonic emissions and easy switching to the RX LNA.

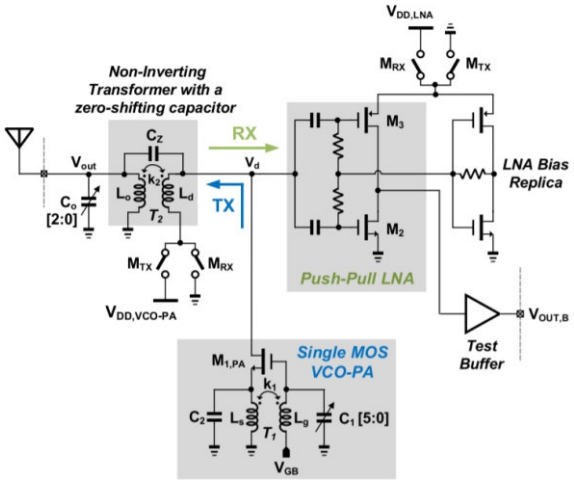


Fig. 1. Schematic of the proposed single-pin antenna interface RF Front End.

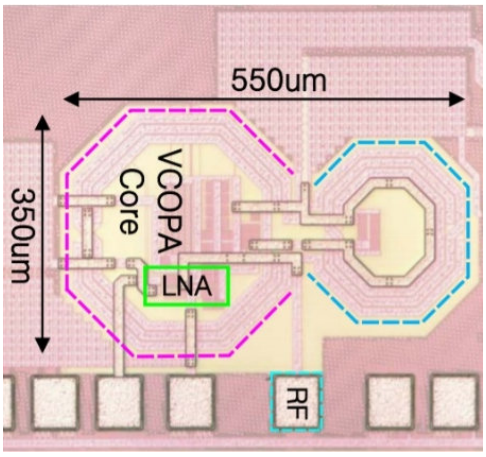


Fig. 2. Chip micrograph.

Publication(s)

[1] K. Xu, J. Yin, P. -I. Mak, R. B. Staszewski, and R. P. Martins, "A Single-Pin Antenna Interface RF Front End Using a Single-MOS DCO-PA and a Push-Pull LNA," IEEE Journal of Solid-State Circuits, pp. 2055-2068, vol. 55, Aug. 2020.

[2] K. Xu, J. Yin, P. -I. Mak, R. B. Staszewski, and R. P. Martins, "A 2.4-GHz Single-Pin Antenna Interface RF Front-End with a Function-Reuse Single-MOS VCO-PA and a Push-Pull LNA," IEEE Asian Solid-State Circuits Conference (A-SSCC), pp. 293-294, Nov. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

An Inverse-Class-F CMOS Oscillator with Intrinsic-High-Q 1st -Harmonic and 2nd -Harmonic Resonances

Chee Cheow Lim, Harikrishnan Ramiah, Jun Yin, Pui-In Mak, and Rui P. Martins

FEATURES

A single-ended PMOS-NMOS-complementary architecture to generate the differential outputs

A transformer tank generates two intrinsic-high-Q resonances at the fundamental frequency F_{LO} and the 2nd-harmonic frequency $2F_{LO}$

Silicon verified in TSMC 65 nm CMOS

A state-of-the-art FoM of 196.1 dBc/Hz at 4 GHz

DESCRIPTION

This work proposes an inverse-class-F (class-F^{-1}) CMOS oscillator. It features: 1) a single-ended PMOS-NMOS-complementary architecture to generate the differential outputs, and 2) a transformer-based 2-port resonator to boost the drain-to-gate voltage gain (A_V) while creating two intrinsic-high-Q impedance peaks at the fundamental (f_{LO}) and double ($2f_{LO}$) oscillation frequencies. The enlarged 2nd-harmonic voltage extends the flat span in which the Impulse Sensitivity Function (ISF) is minimum, and the amplified gate voltage swing reduces the current commutation time, thereby lowering the $-g_m$ transistor's noise-to-phase noise (PN) conversion.

Prototyped in 65-nm CMOS, the class-F^{-1} oscillator at 4 GHz exhibits a PN of –144.8 dBc/Hz at 10 MHz offset while offering a tuning range of 3.5 to 4.5 GHz. The corresponding figure-of-merit (FoM) is 196.1 dBc/Hz, and the die area is 0.14 mm².

Benchmarking with the prior art, our class-F^{-1} CMOS VCO exhibits the highest FOMs at both 100kHz and 10MHz offsets over a comparable tuning range while achieving low frequency pushing.

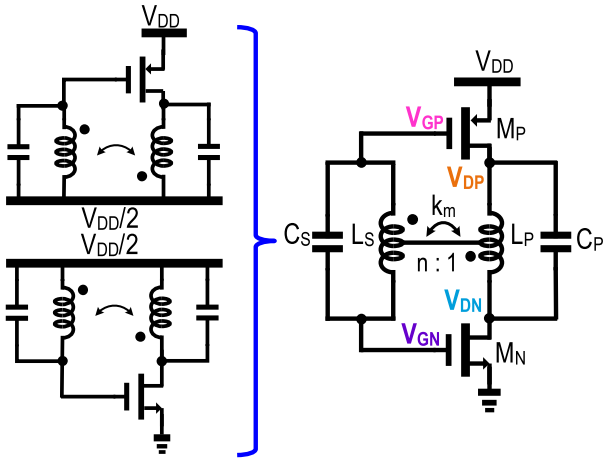


Fig. 1. Class-F-1 oscillator with a PMOS-NMOS-complementary topology to generate the differential outputs.

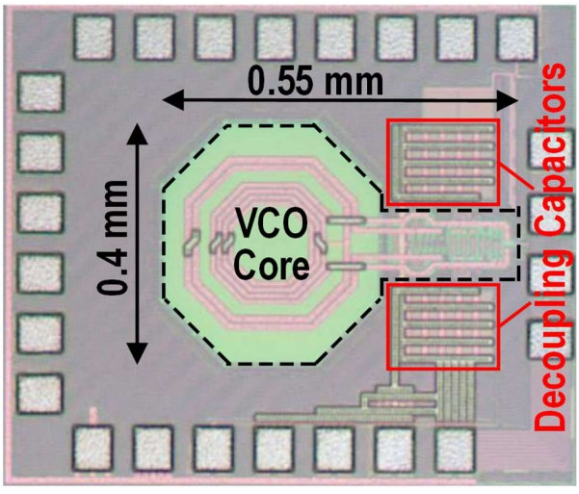


Fig. 2. Chip micrograph.

Publication(s)

[1] C. -C. Lim, H. Ramiah, J. Yin, P. -I. Mak, and R. P. Martins, "An Inverse-Class-F CMOS Oscillator with Intrinsic-High-Q First Harmonic and Second Harmonic Resonances," IEEE Journal of Solid-State Circuits, pp. 3528-3593, vol. 53, Dec. 2018.

[2] C. -C. Lim, J. Yin, P. -I. Mak, H. Ramiah, and R. P. Martins, "An Inverse-Class-F CMOS VCO with Intrinsic-High-Q 1st– and 2nd-Harmonic Resonances for $1/f^2$-to-$1/f^3$ Phase Noise Suppression Achieving 196.2dBc/Hz FoM," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 374-375, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of the University of Macau.

Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools

Ricardo Martins, Nuno Lourenço, Nuno Horta, Shenke Zhong, Jun Yin, Pui-In Mak and Rui P. Martins

FEATURES

A complementary class-B/C hybrid-mode voltage-controlled oscillator (VCO) topology to minimize the power consumption at a standard high supply voltage

A two-step electronic-design-automation-assisted (EDA-assisted) flow to optimize device parameters and generate the layout automatically

Silicon verified in TSMC 65 nm CMOS

Measurement results confirm the effectiveness of the EDA-assisted flow

DESCRIPTION

Optimal VCO design for ultralow-power (ULP) radios has to fulfill simultaneously multiple requirements such as frequency tuning range, phase noise, power consumption, and frequency pushing. The manual design struggles to approach the full potential that a given topology can achieve. This work proves the role of EDA tools by fully supporting the complex design of a ULP complementary Class-B/C hybrid-mode VCO. In the 1st step of the EDA-assisted flow, we perform a worst-case corner of worst-case tuning sizing optimization over a 108-dimensional performance space, offering sizing solutions with power consumption down to 145 µW at the worst-case. In the 2nd step, we introduce an automatic layout generation tool to offer valuable insights into the post-layout design space and devise a ready-for-tape-out fine optimization strategy.

The hybrid-mode VCO designed by the two-step EDA-assisted flow is prototyped in 65-nm CMOS. It occupies a die area of 0.165 mm² and dissipates 297 µW from a 0.8 V supply at 5.1 GHz. The phase noise at 1MHz offset is −110.1dBc/Hz, resulting in a competitive Figure-of-Merit (FoM) of 189.4 dBc/Hz, well-suited for ULP applications.

(a)

(b)

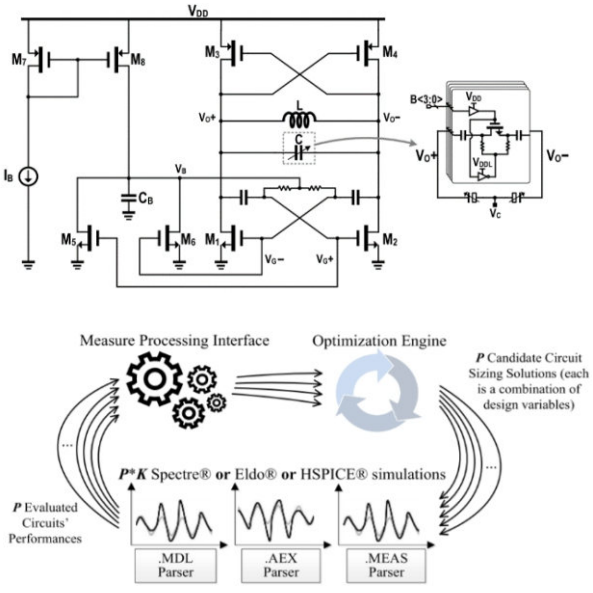
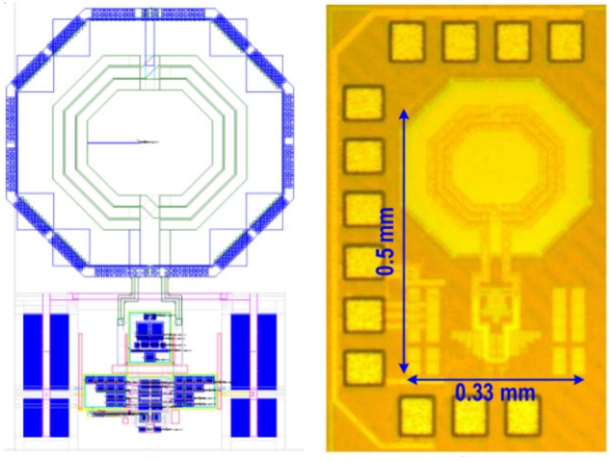


Fig. 1. (a) Complementary class-B/C hybrid-mode VCO topology and (b) flow of multi-test bench analog and RF IC sizing optimization.



(a) (b)

Fig. 2. (a) Automatically generated layout outputted by the EDA tool and (b) chip micrograph.

Publication(s)

[1] R. Martins, N. Lourenço, N. Horta, S. Zhong, J. Yin, P. -I. Mak and R. P. Martins, "Design of a 4.2-to-5.1 GHz Ultralow-Power Complementary Class-B/C Hybrid-Mode VCO in 65-nm CMOS Fully Supported by EDA Tools," IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I), pp. 3965-3977, vol. 67, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

A 0.7-to-2.5 GHz, 61% EIRP System Efficiency, 4-Element MIMO TX Exploiting Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver

Wei-Han Yu, Ka-Fai Un, Pui-In Mak and Rui P. Martins

FEATURES

- Wideband MIMO transmitter (0.7 to 2.5 GHz)
- High EIRP System Efficiency, 61%
- High EIRP average power, 19.2 dBm
- No matching network to avoid power loss
- Analog spatial de-interleaver for 4-channel baseband
- Silicon verified in 65 nm CMOS

DESCRIPTION

It is a 4-element MIMO transmitter (TX) system that features an analog spatial de-interleaver to simplify the baseband-input complexity and increase the spatial matching of the sub-TXs. The MIMO diversity gain and power-combining gain are jointly exploited to relax the output power of the power amplifiers while eliminating their output matching networks, leading to a compact implementation of the entire TX system. The MIMO effectiveness is improved by introducing an RF to baseband DC feedback technique that enhances the matching among the sub-TXs against process variation.

In the verification, the TX system is co-designed with a compact antenna array-on-PCB that generates a null zone in the propagation pattern, and the electric-field polarization angle, to achieve diversity propa-gation. All techniques together improve the signal-to-noise ratio and/or the data rate by generating multiple data streams according to the signal power arriving at the receiver over different fading channels.

Prototyped in 65-nm CMOS, the MIMO TX chip occupies 1.44 mm². It covers an RF range of 0.7–2.5 GHz, and shows an equivalent isotropically radiated power of 23.9 dBm. When transmitting a 20-MHz 64-QAM orthogonal frequency division multiplexing signal at 2.3 GHz, the average system efficiency is 61% and error-vector magnitude is −26 dB.

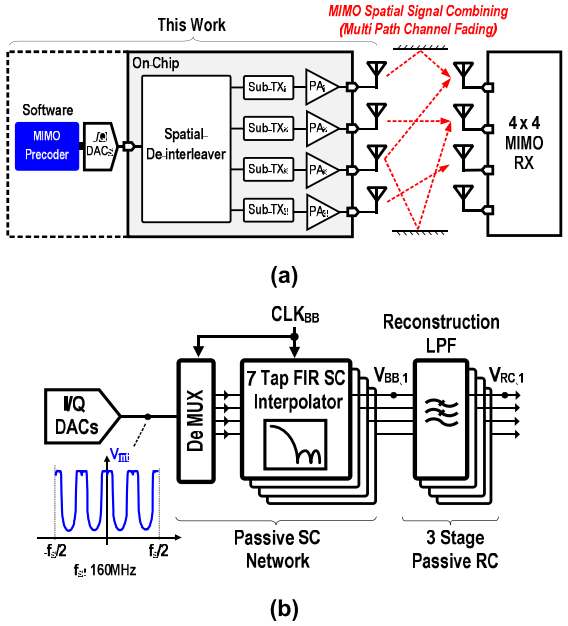


Fig. 1. (a) MIMO TX architecture and (b) analog spatial de-interleaver.

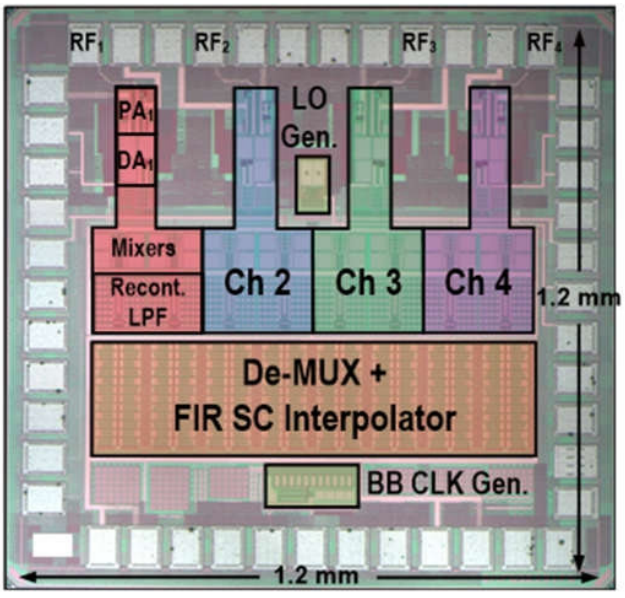


Fig. 2. Chip micrograph.

Publication(s)

[1] W. Yu, K. Un, P. Mak and R. P. Martins, "A 0.7–2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 14-25, Jan. 2018.

Sponsorship

Macao Science and Technology Development Fund SKL Fund and the University of Macau.

A 0.12-mm² 1.2-to-2.4 mW 1.3-to-2.65 GHz Fractional-N Bang-Bang Digital PLL with 8-µs Settling Time for Multi-ISM-Band ULP Radios

Ka-Fai Un, Gengzhen Qi, Jun Yin, Shiheng Yang, IEEE, Shupeng Yu, Chio-In Ieong, Pui-In Mak and Rui P. Martins

FEATURES

Wide frequency range DPLL (1.3 to 2.65 GHz)

Low power consumption, 1.2 to 2.4 mW

Fast settling time, 8 µs

Mismatch-free DTC gain calibration

Split coarse-fine PLL loops with different bandwidth

Silicon verified in 65 nm CMOS

DESCRIPTION

It is a wideband fractional-N bang-bang DPLL for multi-ISM-band ULP radios. To improve the settling time, we proposed two techniques: 1) a mismatch-free DTC gain calibration scheme and 2) split coarse-fine PLL loops. They, together,allow fast startupsettling and channel switching. The employed ring VCO (RVCO) aids to extend the frequency tuning range and generate multi-phase outputs.

Prototyped in 65-nm CMOS, the DPLL consumes 1.2 to 2.4 mW over a wide frequency locking range of 68.3% (1.3 to 2.65 GHz) and occupies a die area of 0.12 mm². The settling time measures 8 µs at an 82-MHz initial frequency error.

Benchmarking with other state-of-the-art fractional PLLs, this work significantly reduces the convergence time of the DTC gain calibration loop, with a settling time that is even faster than an ADPLL only using a TDC.

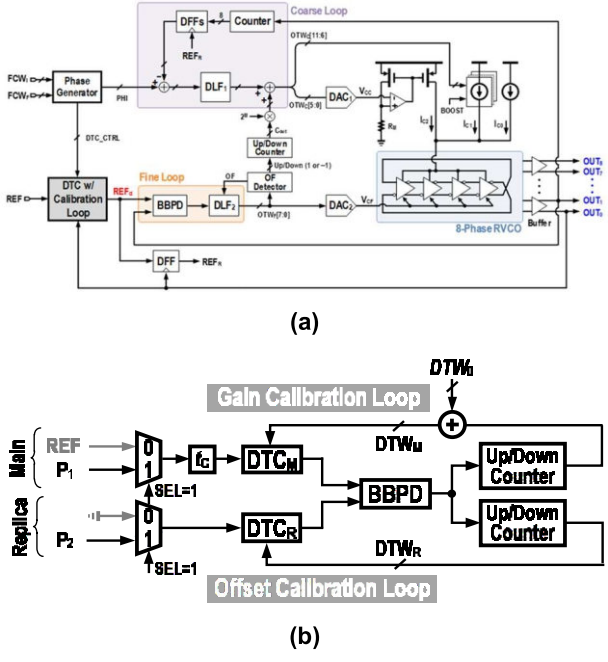


Fig. 1. (a) Digital PLL (RFE) architecture and (b) calibration loop for DTC.

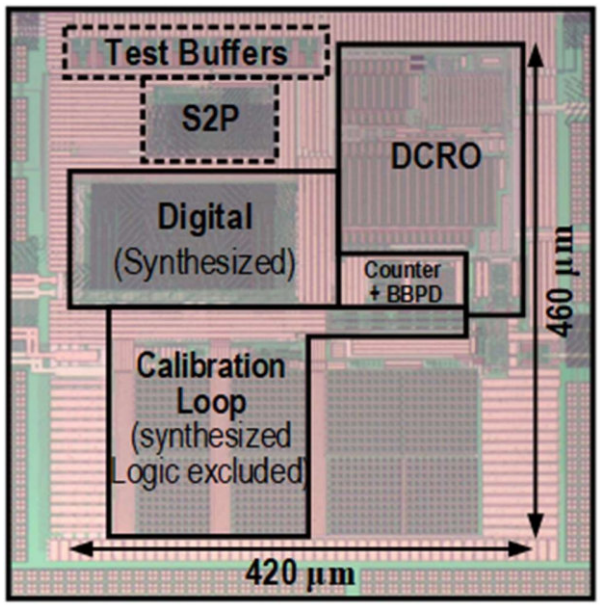


Fig. 2. Chip micrograph.

Publication(s)

[1] K.-F. Un, G. Qi, J. Yin, S. Yang, S. Yu, C.-I. Ieong, P.-I. Mak, and R. P. Martins, "A 0.12-mm² 1.2-to-2.4-mW 1.3-to-2.65-GHz Fractional-N Bang-Bang Digital PLL With 8-µs Settling Time for Multi-ISM-Band ULP Radios," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 9, pp. 3307-3316, Sept. 2019.

Sponsorship

Macao Science and Technology Development Fund SKL Fund and the University of Macau.

Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection

Ka-Fai Un, Feifei Zhang, Pui-In Mak, Rui P. Martins, Anding Zhu and Robert Bogdan Staszewski

FEATURES

Analytical study of interpolative digital transmitter

Procedures for determining sampling rate, resolution, linear interpolation ratio

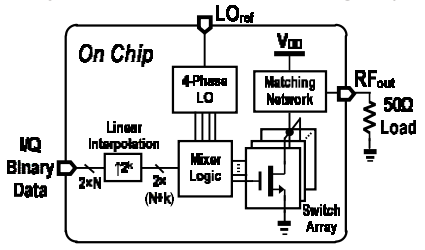
Fulfilling replica rejection and noise floor for different specifications with relaxed high speed digital interface

Improved replica rejection by interpolation, 23 dB

Improved noise floor by interpolation, 2.2 bits

DESCRIPTION

The digital transmitter (DTX) offers both high power efficiency and frequency flexibility by merging signal amplification and modulation in the switching power amplifier. Yet, the back-end high-speed digital baseband interface is challenging and bulky for obtaining low out-of-band noise. This work provides an analytical study of the DTX linear interpolation technique, which can be easily utilized for optimizing the replica rejection and noise-filtering capabilities of the DTX.



(a)

$$H_{2^k}(jf) = \frac{1}{\pi T_s f}\sin(\pi T_s f)\prod_{n=1}^{k}\cos\left(\frac{\pi T_s f}{2^n}\right)$$

Linear Interpolation Rate	1×	2×	4×	8×	16×
Required OSR	50	25	12.5	6.25	5.4
Dominant Replica	1st	2nd	4th	8th	1st

(b)

Fig. 1. (a) Interpolative digital transmitter architecture, and (b) frequency response of the 2^k-step linear interpolator and the dominated replicas.

An IEEE 802.11g orthogonal frequency division multiplexing (OFDM) signal has been generated to verify the derived results, with the sampling frequency chosen to be 120 MHZ. The first replica is suppressed to –24.4/–47.2 dBc without/with interpolation, respectively. The noise floor of 2×11-bit ENOB is –159 dBc/Hz at 95 MHz offset without interpolation while the noise floor of 9-bit ENOB is –160 dBc/Hz at 96 MHz offset with 8× interpolation.

The linear interpolation technique not only can suppress the replicas of the sampling in an RF DTX, but also can lower the quantization noise floor level. The results are supported by quantitative examples by concerning the practical hardware limits at RF. It is revealed that linear interpolation can aid effectively sampling-frequency reduction without sacrificing the replica rejection. It can also relax the resolution of the baseband signal for smaller I/O pin count.

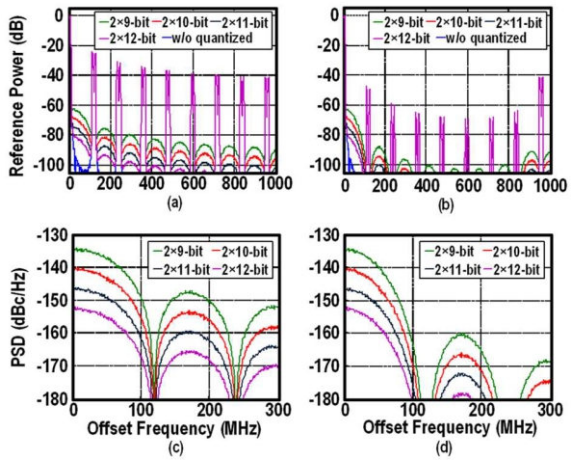


Fig. 2. Replica and noise spectrum without (left)/ with (right) linear interpolation.

Publication(s)

[1] K.-F. Un, F. Zhang, P.-I. Mak, R. P. Martins, A. Zhu and R. B. Staszewski, "Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 37-41, Jan. 2020.

Sponsorship

Macao Science and Technology Development Fund SKL Fund and the University of Macau and Microelectronic Circuits Centre Ireland (MCCI), Cork, Ireland.

A 0.038mm² SAW-less Multiband Transceiver Using an N-Path SC Gain Loop

Gengzhen Qi, Pui-In Mak and Rui P. Martins

FEATURES

SAW-less Multiband Transceiver (TXR)

Small area, 0.038mm²

Using N-Path Switched-Capacitor (SC) Gain Loop as a reconfigurable transmitter (TX) and receiver (RX)

Utilizing Switched-BB-extraction technique in RX mode

Utilizing High-efficiency PA driver (PAD) in TX mode

Fabricated in 65nm CMOS technology

DESCRIPTION

It is a SAW-less compact multiband transceiver (TXR) for LTE standard by employing a switched-capacitor (SC)-Gain Loop that is a negative-gain stage with an SC network as its feedback. Any signals, radio frequency (RF) or baseband (BB), properly injected into the loop will undergo gain, down-mix and up-mix; all are primary functions of transmitter (TX) or receiver (RX). Thus, the SC-gain loop can operate as a basic TX by injecting the BB signal while extracting the RF signal, or a basic RX by injecting the RF signal while extracting the BB signal. This duality suggests the possibility of using the SC-gain loop as a reconfigurable TXR (Fig. 1) appropriate for LTE-TDD. Elegantly, the extra downmix path in the TX and upmix path in the RX allow the SC-gain loop to effectively combine with the gain-boosted N-path technique to realize LO-defined high-Q bandpass (de)modulation.

The TXR fabricated in 65nm CMOS has a die area of 0.038mm² (Fig. 2). For TX mode, the output power shows -1dBm at 1.88GHz (Band2) with -40dBc $ACLR_1$ and 2.0% EVM. The output noise floor is -154.5dBc/Hz at 80MHz offset The TX-mode consumes 31.3mW (Band5) to 38.4mW (Band2). For RX mode, the S_{11} is <–12dB. The NF ranges from 2.2 to 3.2dB. The RF BW reaches to 10MHz. The achieved OB-P_{1dB} (-5dBm) and OB-IIP_3 (+8dBm) are both competitive at 80MHz offset.

Benchmarking with the prior art, the transmitter succeeds in improving the multiband flexibility and area efficiency that is 24x better than the state-of-the-art, while preserving a comparable power efficiency (2.1% for Band2 and 2.4% for Band5); while the receiver succeeds in achieving comparable power consumption, NF and OB-IIP_3.

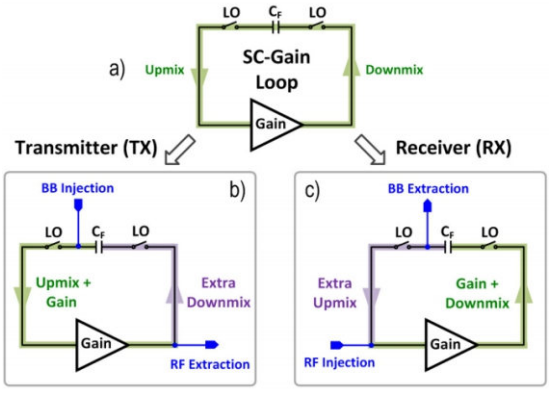


Fig. 1. (a) Switched-capacitor (SC)-Gain Loop. It can operate as a (b) TX under BB-injection RF-extraction, or (c) RX under RF-injection BB-extraction.

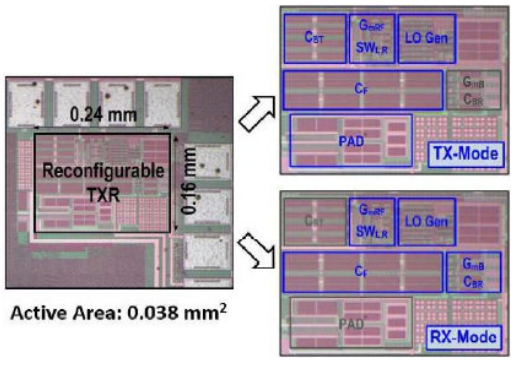


Fig. 2. Chip micrograph.

Publication(s)

[1] G. Qi, P.-I. Mak and R. P. Martins, "A 0.038mm2 SAW-less multi-band transceiver using an N-path SC gain loop," in IEEE Journal of Solid-State Circuits, vol. 52, no. 8, pp. 2055-2070, Aug. 2017.

[2] G. Qi, P.-I. Mak and R. P. Martins, "A 0.038mm² SAW-less multi-band transceiver using an N-path SC gain loop," in IEEE ISSCC Dig. Tech. Papers, Feb. 2016, pp. 452-453.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Multiband FDD SAW-less Transmitter for 5G-NR Featuring a BW-Extended N-Path Filter-Modulator, a Switched-BB Input and a Wideband TIA-Based PA Driver

Gengzhen Qi, Haijun Shao, Pui-In Mak, Jun Yin and Rui P. Martins

FEATURES

Covering 5G-NR FDD bands (1.4 to 2.7GHz)
Low output noise, ≤−157.5dBc/Hz
High transmitter (TX) efficiency, 2.8%–3.6%
Bandwidth-extended N-path filter-modulator
Switched-baseband (BB) input network
TIA-based power amplifier driver (PAD)
Fabricated in 28-nm CMOS technology

DESCRIPTION

An SAW-less transmitter (TX) supporting a 20-MHz BW is proposed in Fig. 1. It aims to cover the 5G-NR FDD bands in the 1.4-to-2.7-GHz range. To balance the performance metrics: channel BW, output noise at small Δf, multiband flexibility, and integration level, three key innovations are featured: 1) a BW-extended N-path filter modulator (BW-Ext FIL-MOD)—it embeds a high-order gain-boosted N-path filter into the I/Q modulator and leads to BW extension and steeper OB filtering; 2) a switched-BB input network—it avoids the mutual loading effect between the BW-Ext FIL-MOD and input network, to uphold a high-Q filtering profile at RF and to reduce the nonlinearity and crosstalk at BB; and 3) a trans-impedance amplifier (TIA)-based PAD—it absorbs the bias and signal currents of the BW-Ext FIL-MOD for better linearity and power efficiency. It also features an inner-parallel Gm linearizer to suppress its third-order cross-intermodulation product (CIM_3).

Fabricated in 28-nm CMOS technology (Fig. 2), the proposed TX manifests a 20-MHz passband BW and a consistently low OB noise (≤−157.5dBc/Hz) for different 5G-NR bands between 1.4 and 2.7GHz. The TX achieves sufficient output power (+3dBm), high TX efficiency (2.8%–3.6%), and high linearity ($ACLR_1$ <-44dBc and EVM <2%). The active area is 0.31mm².

Benchmarking with the prior art, this work manifests several performance advantages, namely, the linearity, OB noise and TX efficiency thanks to the effective BW-Ext FIL-MOD, switched-BB input network and wideband TIA-based PAD.

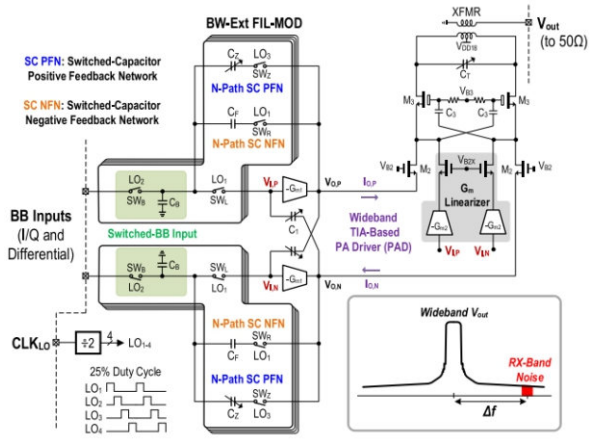


Fig. 1. The fully integrated multiband transmitter (TX) with low receiver (RX)-band noise.

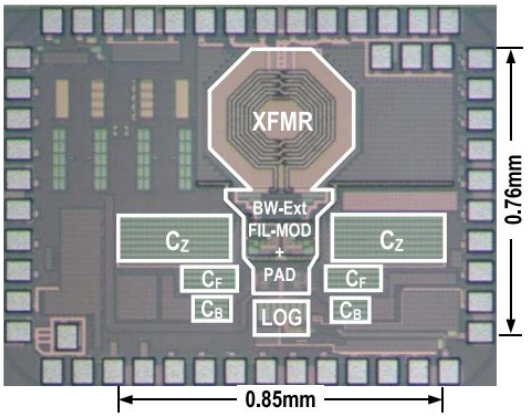


Fig. 2. Chip micrograph.

Publication(s)

[1] G. Qi, H. Shao, P.-I. Mak, J. Yin and R. P. Martins, "A multiband FDD SAW-less transmitter for 5G-NR featuring a BW-extended N-path filter-modulator, a switched-BB input and a wideband TIA-based PA driver," in IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3387-3399, Dec. 2020.

[2] G. Qi, H. Shao, P.-I. Mak, J. Yin, . P. Martins, "A 1.4-to-2.7GHz FDD SAW-less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, an Isolated-BB Input and a Wideband TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise" IEEE ISSCC Dig. Tech. Papers, pp. 172-174, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A SAW-less Tunable RF Front-End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA

Gengzhen Qi, Barend van Liempd, Pui-In Mak, Rui P. Martins and Jan Craninckx

FEATURES

SAW-less tunable RF-FE for 3GPP bands (0.7 to 1GHz)

High TX-RX isolation, >50dB tunable rejection

The first to achieve <-100dBm IM_3 at +20dBm TX power

The first to handle >+30dBm in-band TX power

Large-signal handling switched-LC N-path LNA

Fabricated in 0.18-µm SOI CMOS technology

DESCRIPTION

A SAW-less tunable RF-front end (RF-FE) prototype (Fig. 1) is proposed that integrates the gain-boosted (GB) switched-LC N-path LNA of together with the electrical-balance duplexer (EBD). The EBD cancels the transmitter–receiver (TX–RX) leakage at the RX frequency by dynamically optimizing the balance of a hybrid transformer, which enables in-band full-duplex (IBFD) operation. A transconductor-based LNA in parallel with a switched-LC N-path network creates input and output notches to reject TX leakage for frequency-division duplexing (FDD) operation. The LNA's signal-handling capability is enhanced via optimum switch biasing. This technique enables high linearity, better large-signal handling capability, and dual-frequency TX-to-RX isolation.

Fabricated in 0.18-µm SOI CMOS (Fig. 2), the RF-FE shows >50-dB tunable rejection from the TX input to the LNA output at both TX and RX frequencies, for all 3GPP bands from 0.7 to 1GHz. It is the first tunable RF-FE including an LNA that achieves +70-dBm TX-path IIP_3 and <−100-dBm IM_3 at +20-dBm TX power when a full-duplex spaced (FDS) jammer is applied at the antenna (FDD case) and the first that handles >+30-dBm in-band TX power while providing >50-dB self-interference cancellation (IBFD case). It consumes 62.5mW operating at 1GHz with 11.7-dB RX cascaded NF and 3.6-dB TX insertion loss, and occupies 9.62mm² active area.

This work features a highly integrated RF-FE for FDD and IBFD operations, meanwhile achieving comparable performances on TX-RX isolation, OB-IIP_3, OB-iB_{1dB} and NF etc., when benchmarked with the state-of-the-art works.

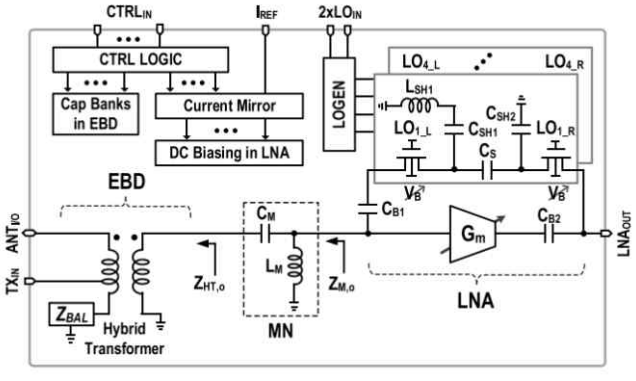


Fig. 1. High integrated RF- front end (RF-FE) using an electrical-balance duplexer (EBD) and a switched-LC N-path low-noise amplifier (LNA).

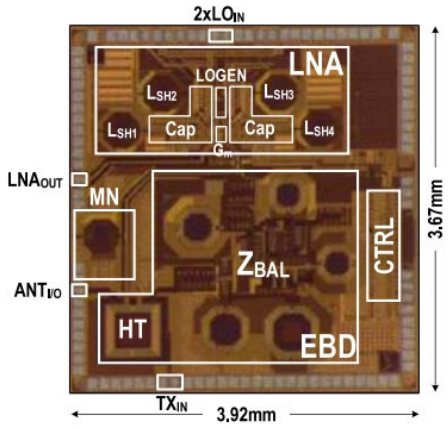


Fig. 2. Chip micrograph.

Publication(s)

[1] G. Qi, B. van Liempd, P.-I. Mak, R. P. Martins and J. Craninckx, "A SAW-less tunable RF front-end for FDD and IBFD combining an electrical-balance duplexer and a switched-LC N-path LNA," in IEEE Journal of Solid-State Circuits, vol. 53, no. 5, pp. 1431-1442, May. 2018.

[2] G. Qi, B. van Liempd, P.-I. Mak, R. P. Martins and J. Craincks, "0.7-1 GHz LO-defined SAW-less LNA for FDD using SOI CMOS technology," in IEEE Radio Frequency Integrated Circuits Symposium (RFIC), Jun. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.096-mm² 1–20-GHz Triple-Path Noise Canceling Common-Gate Common-Source LNA With Dual Complementary pMOS–nMOS Configuration

Haohong Yu, Yong Chen, Chirn Chye Boon, Pui-In Mak, and Rui P. Martins

FEATURES

Common-gate common-source LNA

Triple-path noise canceling

Dual complementary pMOS-nMOS configuration

Silicon verified in 65nm CMOS

DESCRIPTION

We propose a novel wideband common-gate (CG) common-source (CS) low-noise amplifier (LNA) with a dual complementary pMOS–nMOS configuration to provide a current-reuse output. Triple-path noise-cancellation is revealed to eliminate the thermal noise of the two CG transistors. Simultaneously, partial cancellation of intrinsic third-order distortion of output-stage transistors improves the input third-order intercept point (IIP3). In addition, we embed a resistive feedback in one of the auxiliary CS amplifiers to balance the multiple tradeoffs between noise figure (NF), input matching (S_{11}), and forward gain (S_{21}).

Fabricated in 65-nm CMOS, the proposed wideband LNA exhibits an IIP3 of 2.2–6.8 dBm and an NF of 3.3–5.3 dB across a 19-GHz BW while consuming 20.3 mW at 1.6 V. S11 is <−10 dB up to 23 GHz by designing a π-type inputmatching network. The LNA exhibits a peak S21 of 12.8 dB and occupies a very compact die area of 0.096 mm².

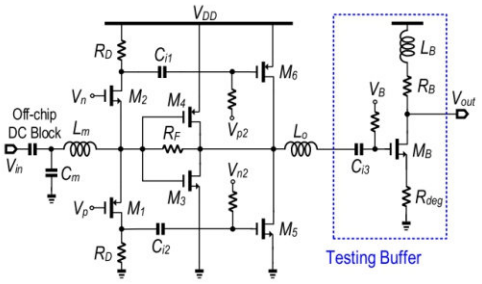


Fig. 1. Complete schematic of our wideband LNA.

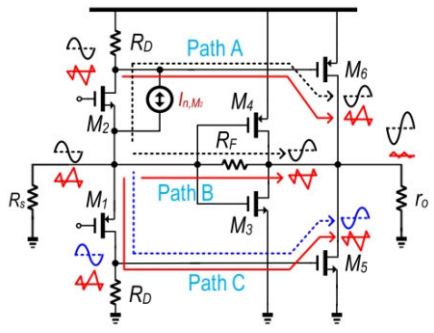


Fig. 2. Overall triple-path NC mechanism.

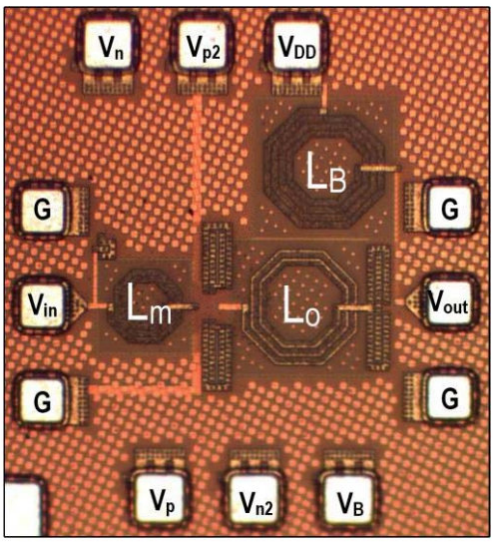


Fig. 3. Die photograph of the fabricated wideband LNA.

Publication(s)

[1] H. Yu, Y. Chen, C. C. Boon, P.-I. Mak, and R. P. Martins, "A 0.096-mm² 1-to-20-GHz Triple-Path Noise-Cancelling Common-Gate Common-Source LNA with Complementary pMOS-nMOS Configuration," IEEE Transactions on Microwave Theory and Techniques, vol. 68, pp. 144-159, Jan. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled MM-Wave VCO Using a Single-Center-Tapped Switched Inductor

Yatao Peng, Jun Yin, Pui-In Mak and Rui P. Martins

FEATURES

An inductive mode-switching technique to vary the effective tank inductance without compromising the tank quality factor

Coupling four voltage-controlled-oscillator (VCO) cores for phase noise reduction

Silicon verified in TSMC 65 nm CMOS

A state-of-the-art peak FoM of 186.6 dBc/Hz at 50 GHz

DESCRIPTION

This work proposes a mode-switching quad-core-coupled millimeter-wave (mm-Wave) VCO, using an inductive mode-switching technique to extend the frequency tuning range and improve the phase noise. The switches not only serve for in-phase coupling among the VCO cores but also can modify the equivalent tank inductance suitable for coarse frequency tuning. The frequency gaps between the multi-resonant frequencies are controlled by the common-mode (CM) inductance LCM precisely set by the lithography fabrication. Together with the tiny varactors for fine frequency tuning, a wide and continuous frequency tuning range can be achieved. It is analytically shown that tiny switches (i.e., small parasitic capacitance) for mode selection are adequate to avoid bimodal oscillation, synchronize the VCO cores against resonance frequency mismatches, and prevent PN degradation. A symmetrical layout of a single-center-tapped switched inductor also aids the VCO to be immune to magnetic pulling

Prototyped in 65-nm CMOS, our VCO exhibits a 16.5% tuning range from 42.9 to 50.6 GHz. The phase noise at 50 Ghz is −115.6 dBc/Hz at 3-MHz offset, corresponding to a figure-of-merit (FoM) of 183.6 dBc/Hz. The die size is 0.039 mm²

Benchmarking with the prior fundamental VCOs operating above 40GHz, our design exhibits the best-in-class phase noise and FOM.

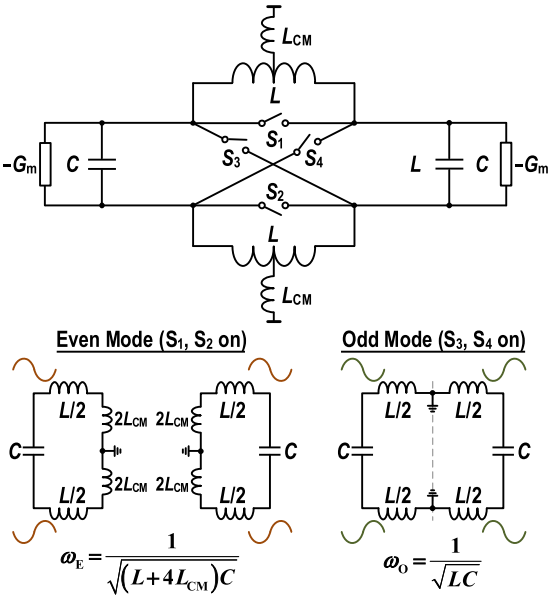


Fig. 1. Proposed inductive mode-switching technique.

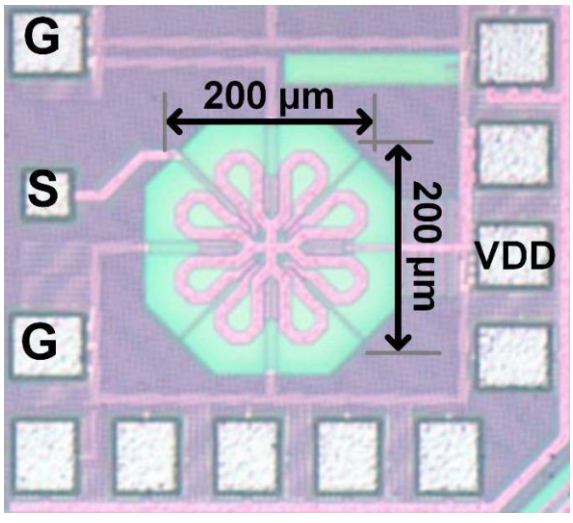


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Peng, J. Yin, P. -I. Mak, and R. P. Martins, "Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled mm-wave VCO Using a Single-Center-Tapped Switched Inductor," IEEE Journal of Solid-State Circuits, pp. 3232-3242, vol. 53, Nov. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of the University of Macau.

RESEARCH ABSTRACTS

Wireline Integrated Circuits

A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS -------- 25

A 0.08mm² 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6 dBc/Hz FOM and 130kHz 1/f³ PN Corner -------- 26

A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS -------- 27

A 0.0018-mm² 153% Locking-Range CML-Based Divider-by-2 With Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell -------- 28

A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-Only Switched-Capacitor Arrays With a 187.6-dBc/Hz FOM -------- 29

A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning -------- 30

A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers With Maximized Timing Margin -------- 31

An Area-Efficient and Tunable Bandwidth Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling -------- 32

A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS

Chao Fan, Wei-Han Yu, Pui-In Mak, Rui P. Martins

FEATURES

SCH output wireline driver

FFE support

PAM-4 modulated TX

High throughput, 10 Gb/s

Low energy consumption, 0.16 pJ/bit

Silicon verified in TSMC 28nm CMOS

DESCRIPTION

This work proposes an SST-CML-Hybrid (SCH) output driver, and its corresponding hybrid-path feed-forward equalization (FFE) scheme, to enhance the energy efficiency of a PAM-4 transmitter (TX). Specifically, the SCH driver features one SST branch + one CML branch to co-synthesize the PAM-4 data, reducing substantially the signaling power, switching power and equalization power. The PAM-4 TX further integrates a half-rate serializer with 4-bit 3-tap FFE, duty-cycle correction circuits and a T-coil output matching network. Prototyped in 28-nm CMOS, the PAM-4 TX achieves a broadband return loss <; -10dB up to 50 GHz, and occupies a compact die area of 0.0345 mm². Operating at 40 Gb/s and at a 0.9-V supply, the TX dissipates 19.5 mW, of which 6.4 mW is due to the SCH driver. The corresponding energy efficiencies are 0.16 and 0.5 pJ/bit for the SCH driver and TX, respectively; both compare favorably with the prior art

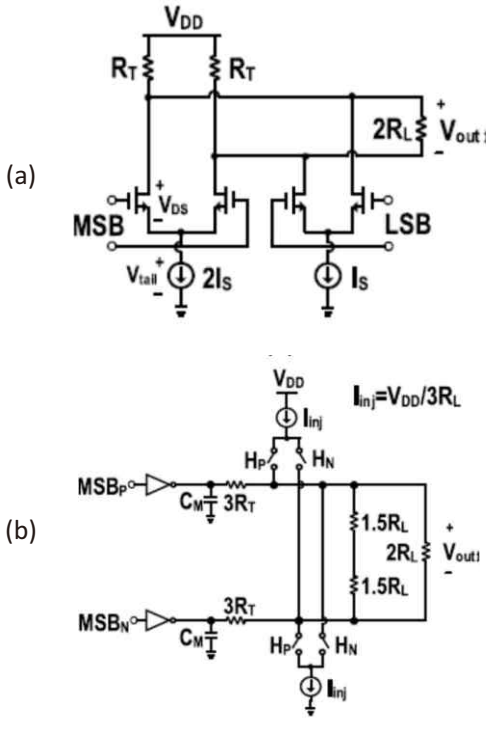


Fig. 1. (a) Conventional CML, and (b) proposed SCH PAM-4 driver.

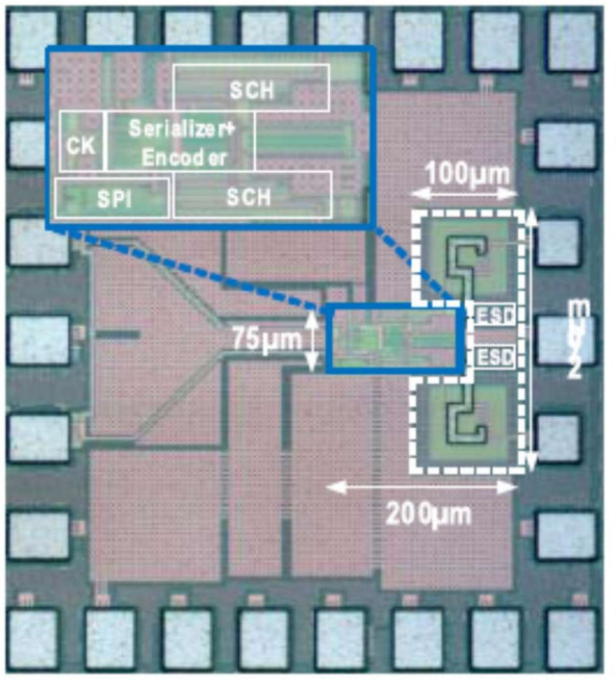


Fig. 2. Chip micrograph.

Publication(s)

[1] Chao Fan, Wei-Han Yu, Pui-In Mak, Rui P. Martins, "A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS," IEEE Transactions on Circuits and Systems – I, vol. 66, pp. 4850-4861, Dec. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 0.08mm² 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6 dBc/Hz FOM and 130kHz 1/f³ PN Corner

Hao Guo, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

Multi-resonant-RLCM-tank VCO

Single-turn multi-tap inductor with high-Q 1st-, 2nd- and 3rd-harmonic resonances

Remove the constraint of the DM-to-CM capacitance ratio with CM-only tunable capacitors

Significantly suppress the transistor noise to phase noise conversion

Silicon verified in 65nm CMOS

DESCRIPTION

We report a near-millimeter-wave VCO using a multi-resonant RLCM tank that enables compact and high-FoM implementation. Specifically, a single turn multi-tap inductor with k<0 and CM-only tunable capacitors, without the constraint of the DM-to-CM capacitance ratio, enable high-Q high-impedance resonances at different oscillation frequencies (e.g., F_{OSC}, $2F_{OSC}$, and $3F_{OSC}$.

Our VCO was prototyped in 65nm CMOS. The active and capacitive elements are laid out inside the inductor footprint for area savings. With our tunable capacitance range and resolution, the PN and FoM after manual resonance alignment is 5dB (8dB) better at a 1MHz (100kHz) offset. When operating in a PLL, C_{CM} can be tuned for frequency locking first, then C_2 to optimize the PN performance.

Benchmarking with the recent mm-wave VCOs, this work succeeds in improving both FoM and FoM_T over a wide range of frequency offsets. We also achieve a low 1/f³ PN corner and a small core area. Measuring a TR of 16% from 25.5 to 29.9GHz, our VCO achieves a FoM@1MHz up to 191.6dBc/Hz that is at least 2dB better than the prior art mm-wave VCOs in both CMOS and BiCMOS.

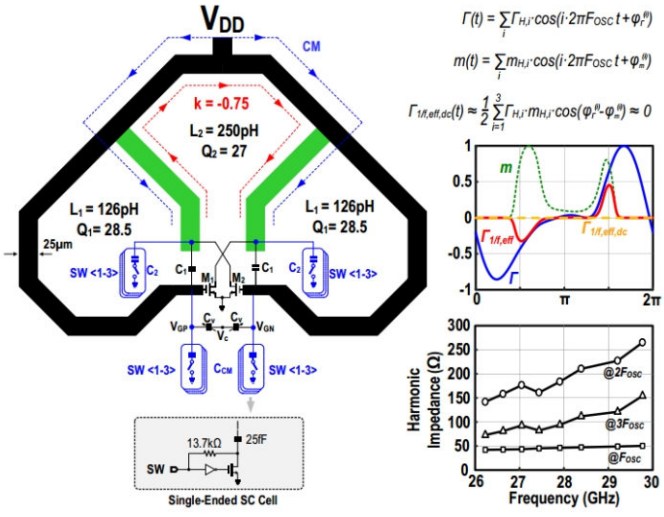


Fig. 1. Left: Proposed compact single-turn multi-tap inductor with high Q_1 and Q_2. Right: Simulated Γ, m and $\Gamma_{1/f,eff}$ in one cycle and harmonic impedances over TR.

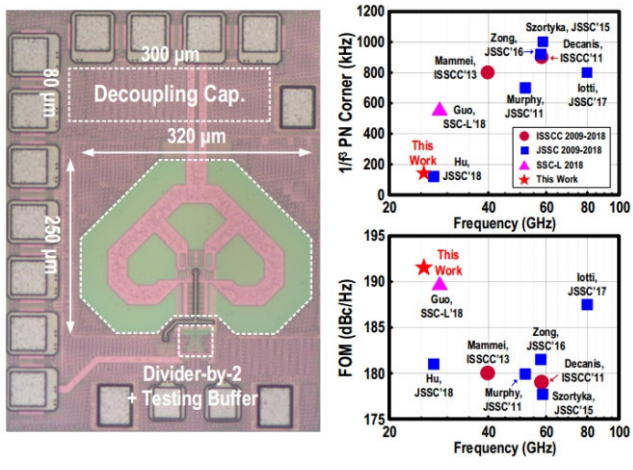


Fig. 2. Left: Die photo of the fabricated mm-wave VCO in 65nm CMOS. Right: Plots of FOM and 1/f³ PN corner with respect to more state-of-the-art mm-wave VCOs.

Publication(s)

[1] H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.08mm2 25.5-to-29.9GHz Multi-Resonant-RLCM-Tank VCO Using a Single-Turn Multi-Tap Inductor and CM-Only Capacitors Achieving 191.6-dBc/Hz FOM and 130kHz 1/f³ PN Corner," IEEE International Solid-State Circuits Conference (ISSCC), pp. 410-411, Feb. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS

Xiaoteng Zhao, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

Half-rate bang-bang clock and data recovery circuit

Trimodal (NRZ/PAM-4/PAM-8)

Single-loop phase tracking technique

Silicon verified in 65nm CMOS

DESCRIPTION

We develop a half-rate bang-bang clock and data recovery (BBCDR) circuit supporting the trimodal (NRZ/PAM-4/PAM-8) operation. The observation of their crossover points distribution at the transitions introduces the single-loop phase tracking technique. In addition, low-power techniques at both the architecture and circuit levels are employed to greatly improve the overall energy efficiency and multiply data throughput by increasing the number of levels on the magnitude.

Fabricated in 28-nm CMOS, our prototype scores a 0.29/0.17/0.14 pJ/bit efficiency at 14.4/28.8/43.2 Gb/s under NRZ/PAM-4/PAM-8 modes, respectively. The jitter is <0.53 ps (integrated from 100 Hz to 1 GHz) with approximately-equivalent constant loop bandwidth, and we achieve at least 1-UI_{pp} jitter tolerance up to 10 MHz for all three modes.

Benchmarking this work with the recent state-of-the arts, we first design a trimodal (NRZ/PAM-4/PAM-8) BBCDR circuit and exhibit favorable energy efficiency (0.14 to 0.29 pJ/bit) and integrated jitter (0.48 to 0.53 ps).

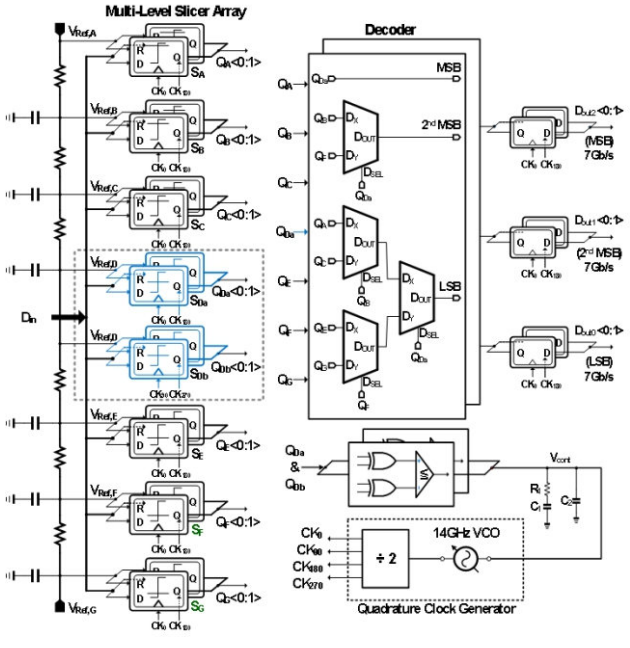


Fig. 1. Complete schematic of our trimodal BBCDR.

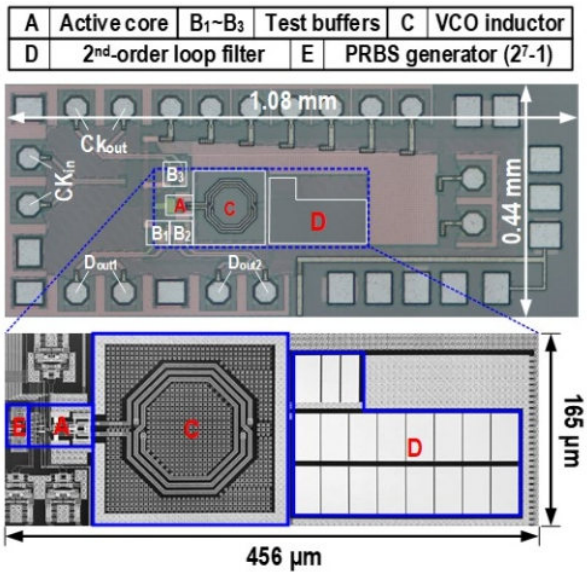


Fig. 2. Chip photo with area breakdown and detail of the core layout.

Publication(s)

[1] X. Zhao, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.14-to-0.29-pJ/bit 14-GBaud/s Trimodal (NRZ/PAM-4/PAM-8) Half-Rate Bang-Bang Clock and Data Recovery (BBCDR) Circuit in 28-nm CMOS," IEEE Transactions on Circuits and Systems - I, vol. 68, pp. 89-102, Jan. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 0.0018-mm² 153% Locking-Range CML-Based Divider-by-2 With Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell

Xiaoteng Zhao, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

CML-based divider-by-2

Tunable self-resonant frequency using an auxiliary negative-g_m cell

Silicon verified in 65nm CMOS

DESCRIPTION

High-performance radio frequency to millimeter-wave frequency dividers are the cornerstone of advanced local-oscillator generators for the 5th-generation (5G New Radio,and clock synchronization in the wireline and optical transceivers.

We report an area-efficient current-mode logic (CML)-based divider, with a tunable self-resonant frequency for locking range (LR) extension.

Specifically, a negative-g_m (NG) cell is inserted between the resonated shunt-peaking inductor and the load resistor to shift the divider's sensitivity curve (SC), enabling concurrently a higher operating frequency and a wider LR. We use the injection-locking concept, together with a graphical phasor diagram with the frequency-phase information to systematically explain the LR-extension mechanism.

Prototyped in a 65-nm CMOS, the divider occupies a tiny active area of 0.0018 mm². The measured LR is 153% (4–30 GHz) while consuming 4.06–4.28 mW at 30 GHz under a single 1.2-V supply.

Comparing the performance of the proposed divider with the state-of-the-art. This work succeeds in enhancing the flexibility of f_{SR} with an LR of 153% to achieve good figure of-merits: FOM_{Pdc} of 25.5 dB and FOM_P of 71.5.

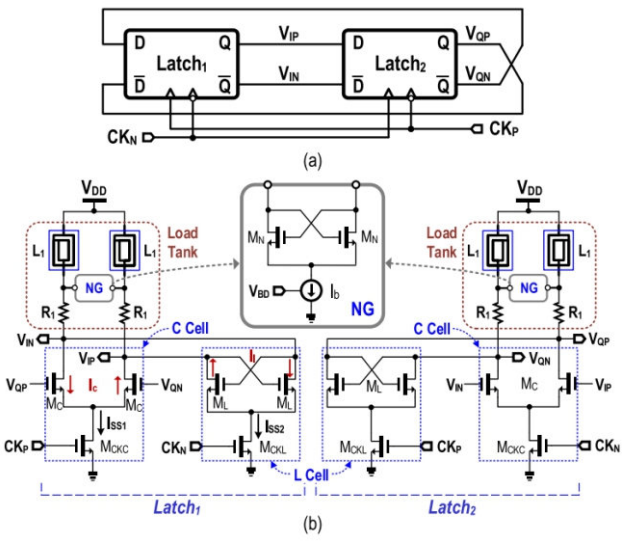


Fig. 1. (a) Two latches view and (b) detailed schematic of our proposed CML-based frequency divider-by-2.

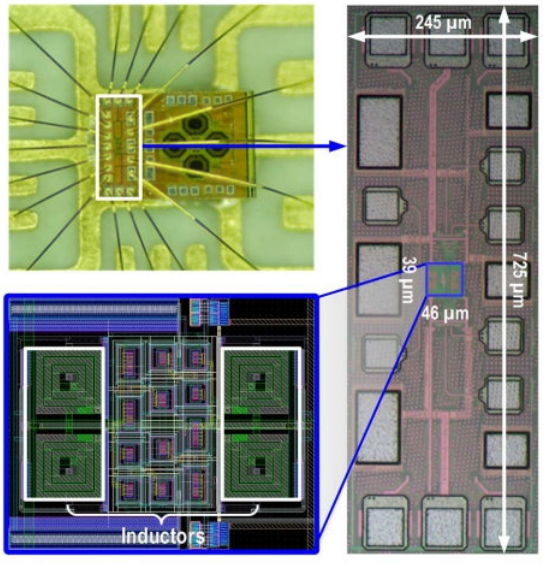


Fig. 2. Chip micrograph with bonding scheme and core layout detail.

Publication(s)

[1] X. Zhao, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.0018-mm² 153%-Locking-Range CML-Based Divider-by-2 with Tunable Self-Resonant Frequency Using an Auxiliary Negative-g_m Cell," IEEE Transactions on Circuits and Systems - I, vol. 66, pp. 3330-3339, Sep. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-Only Switched-Capacitor Arrays With a 187.6-dBc/Hz FOM

Yunbo Huang, Yong Chen, Hao Guo, Pui-In Mak, and Rui P. Martins

FEATURES

Current-reused VCO

Single-turn multi-tap inductor

Differential-only switched-capacitor arrays

Silicon verified in 65nm CMOS

DESCRIPTION

A millimeter-wave current-reuse voltage-controlled oscillator (VCO) features a single-turn multi-tap inductor and two separate differential-only switched-capacitor arrays to improve the power efficiency and phase noise (PN). A single-branch complementary VCO in conjunction with a multi-resonant resistor-inductor-capacitor-mutual inductance (RLCM) tank allows sharing the bias current and reshaping the impulse-sensitivity-function. The latter is based on an area-efficient RLCM tank to concurrently generate two high-quality factor differential-mode resonances at the 1st and 2nd-harmonic oscillation frequencies. and the core area is 0.116 mm².

Fabricated in 65-nm CMOS technology, our VCO at 27.7 GHz shows a PN of −109.91-dBc/Hz at 1-MHz offset (after on-chip divider-by-2), while consuming just 3.3 mW at a 1.1-V supply. It corresponds to a Figure-of-Merit (FOM) of 187.6 dBc/Hz. The frequency tuning range is 15.3% (25.2 to 29.4 GHz) and the core area is 0.116 mm².

Benchmarking with the prior arts, the current-reuse scheme allows our VCO to obtain a competitive FOM (187.4 dBc/Hz ±0.2 dB) at 1-MHz offset with the lower power (<3.5 mW) across the entire 15.3% TR.

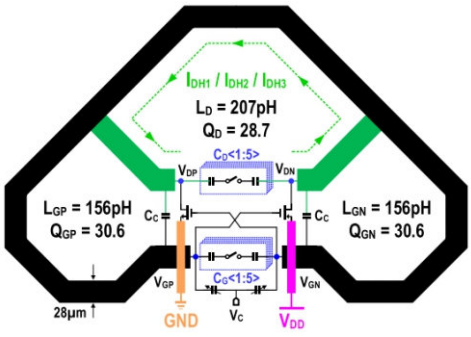


Fig. 1. Schematic of the proposed current-reuse VCO.

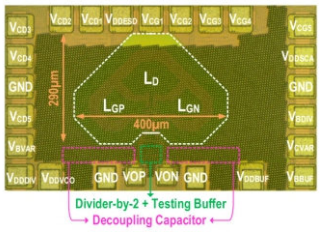


Fig. 2. Chip photo of the designed current-reuse VCO.

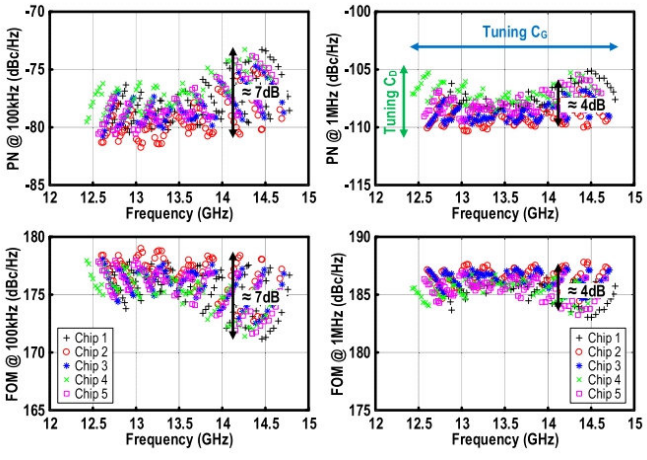


Fig. 3. Multi-chip tests for different SCAs settings.

Publication(s)

[1] Y. Huang, Y. Chen, H. Guo, P.-I. Mak, and R. P. Martins, "A 3.3-mW 25.2-to-29.4-GHz Current-Reuse VCO Using a Single-Turn Multi-Tap Inductor and Differential-only Switched-Capacitor Arrays with a 187.6-dBc/Hz FOM," IEEE Transactions on Circuits and Systems - I, vol. 67, pp. 3704-3717, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning

Hao Guo, Yong Chen, Pui-In Mak, and Rui P. Martins

FEATURES

Wideband-harmonic-shaping VCO

A tiny-coil head resonator for CM bandwidth extension

Wideband 1/f³ PN corner reduction without harmonic tuning

Silicon verified in 65nm CMOS

DESCRIPTION

We present a wideband-harmonic-shaping VCO that exhibits concurrently a high FoM and wideband 1/f3 PN-corner reduction without manual harmonic tuning. We devise a multi-LC tank with a high-and-wideband CM resonance at $2F_{OSC}$ and a low-and-wideband DM resonance at $3F_{OSC}$. To explain later, this scheme optimally shapes the ISF noise transfer over the wide TR from both the magnitude and phase perspectives. The key elements are a 1:2-turn transformer, a tiny coil head resonator (HR), and a switched-capacitor array (SCA) for one-dimensional frequency tuning.

The VCO fabricated in 65nm CMOS occupies a 0.24 mm2 core area. The $PN_{@10MHz}$ is -149dBc/Hz at F_{min}, and -146.1dBc/Hz at F_{max}, resulting in a $FoM_{@10MHz}$ of 195.1dBc/Hz at F_{min} and 196.9dBc/Hz at F_{max}. The corresponding 1/f³ PN corner increases from 90 to 180kHz due to AM-PM conversion, which identifies the corner frequency within a 3dB FoM degradation from $FoM_{@10MHz}$.

Benchmarking with other RF VCOs that exploit the narrowband resonance at $2F_{OSC}$, this work features a wideband high-impedance $|Z_{CM}|$ allowing $FoM_{@10MHz}$ improvement without manual harmonic tuning, while showing less 1/f³ PN corner variation. Specifically, our VCO shows a better $FoM_{@10MHz}$, covers a wider TR of 23.9% and operates at a much lower supply voltage of 0.4V. Compared to the prior work that uses no harmonic tuning, our VCO exhibits a smaller variation of $FoM_{@10MHz}$ of 1.8dB and 1/f³ PN corner of 90kHz over the respective TRs.

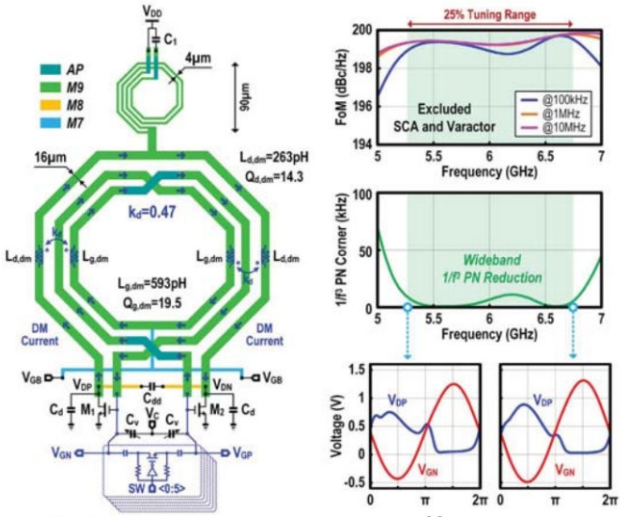


Fig. 1. Left: Detail of the proposed complete VCO. Right: Wideband FoM and 1/f³ PN-corner reduction without manual harmonic tuning.

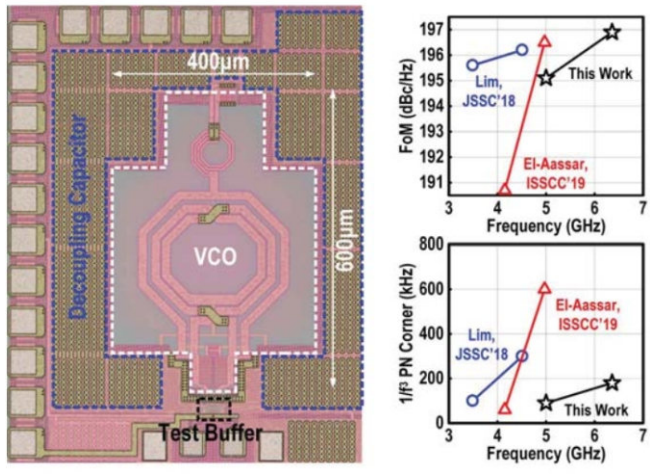


Fig. 2. Left: Die micrograph of the fabricated VCO in 65nm CMOS. Right: Plots of the FoM and 1/f³ PN corner with respect to the prior-art RF VCOs.

Publication(s)

[1] H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 5.0-to-6.36GHz Wideband-Harmonic-Shaping VCO Achieving 196.9 dBc/Hz Peak FoM and 90-to-180kHz 1/f³ PN Corner Without Harmonic Tuning," IEEE International Solid-State Circuits Conference (ISSCC), pp. 294-295, Feb. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT)—SKL Fund; Research Committee of University of Macau (MYRG2017-00223-AMSV).

A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers With Maximized Timing Margin

Yong Chen, Pui-In Mak, Chirn Chye Boon, and Rui P. Martins

FEATURES

Duobinary-signal transmitter

Power-efficient cross-quadrature clocking MUX

Maximized timing margin technique

Silicon verified in 65nm CMOS

DESCRIPTION

For wireline transmitters delivering a high-speed multi-level signal, such as four-level pulse-amplitude-modulation or duobinary, a high-performance multipl-exzer (MUX) is critical to serialize the low-speed parallel data into one full-speed output. To enhance the power efficiency and data eye's opening, this paper proposes a universal 2-to-1 MUX, featuring a cross-quadrature clocking technique to enlarge the timing margin, and a simplified three-latch topology without delay buffers to boost the internal bandwidth (BW). The MUX ratios are extendable to 4-to-2 and 4-to-1, and their benefits are exemplified via a duobinary-signal transmitter. It further includes an output driver unifying the MUX-and-SUM operation, a BW-extended single-to-differential converter, and an active-inductor-embedded clock buffer for swing enhancement. A predictive method for estimating the duobinary-signal data-dependent jitter according to the load capacitance of the output driver is developed.

Fabricated in 65-nm CMOS, the transmitter exhibits a figure-of-merit (FOM) of 1.3 mW/Gb/s at 36 Gb/s, while occupying a compact die area of 0.037 mm².

Benchmarking with the prior art, this work succeeds in improving the FOM and data eye opening by averting several power-hungry blocks, while operating the transmitter in the current domain to maximize the internal BW. It is possible to reduce the power consumption further by migrating this work to a more advanced process (e.g. 28-nm CMOS), resulting in lower power consumption in the clock path. Also, replacing the 2-latch+ 2-DFF array with high-speed digital circuits and employing the power-efficient divider-by-2 are prospective.

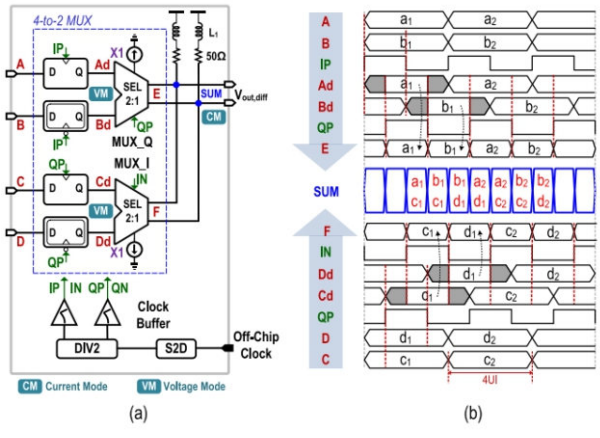


Fig. 1. (a) Top architecture of the proposed duobinary-signal transmitter. (b) Its timing diagram showing the maximum timing margin at every MUX stage.

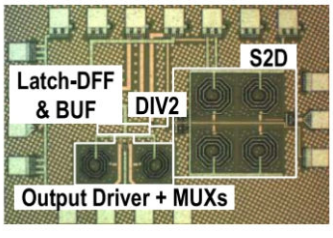


Fig. 2. Die photo of the duobinary-signal transmitter.

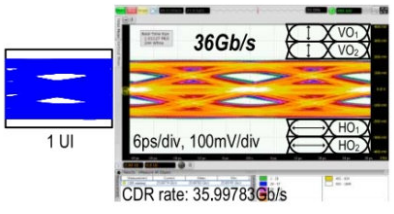


Fig. 3. Simulated (left) and measured (right) eye diagrams of the duobinary-signal transmitter at 36 Gb/s.

Publication(s)

[1] Y. Chen, P.-I. Mak, C. C. Boon, and R. P. Martins, "A 36-Gb/s 1.3-mW/Gb/s Duobinary-Signal Transmitter Exploiting Power-Efficient Cross-Quadrature Clocking Multiplexers with Maximized Timing Margin," IEEE Transactions on Circuits and Systems - I, vol. 65, pp. 3014-3026, Sept. 2018.

Sponsorship

Research Committee of University of Macau (MYRG2017-00223-AMSV).

An Area-Efficient and Tunable Bandwidth Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling

Yong Chen, Pui-In Mak, Haohong Yu, Chirn Chye Boon, and Rui P. Martins

FEATURES

Area-efficient and tunable BW-extension technique

High BWER with only one inductor

Wideband amplifier handling 50+Gb/s signaling

Silicon verified in 65nm CMOS

DESCRIPTION

It is an area-efficient and tunable bandwidth (BW) extension technique for a wideband CMOS amplifier to handle very high rate (50+ Gb/s) signaling. Its architectural advantages are identified by correlating the performances with the frequency domain [magnitude and group delay (GD) responses] and time domain (impulse and step responses) and comparing them with the existing solutions. Specifically, our technique enables a flexible ac characteristic by introducing a tunable grounded active inductor in the bridged-shunt peaking topology, offering: 1) a high BW enhancement ratio (BWER = 2.65×); 2) BW-power scalability with small in-band gain variation; and 3)fine tunability of the passband gain without affecting the BW, GD, and power.

The experimental prototype is a 65-nm CMOS four-stage differential amplifier occupying just 0.0077 mm2. It delivers a 15-dB gain over a 43-GHz BW with 45-mW power consumption. Small in-band gain variation (0.58 dB) and ripple (1.53 dB) are concurrently achieved with low in-band GD variation (17 to 35.3 ps) and ripple (18.3 ps). The achieved figure of merit of 5.48 [(dc Gain×BW) / Power] compares favorably with the prior art.

Benchmarking with the prior art, this work succeeds in enhancing the flexibility of the ac characteristics, while achieving a better FOM and area efficiency. This work realizes tunability by varying k_g in the current domain and k_v in the voltage domain with a little expense of in-band gain variation. In addition, differing from other works that employ more than two passive inductors along the signal path, causing more coupling and parasitics, this work extends BW by adding a GAI as an independent auxiliary path.

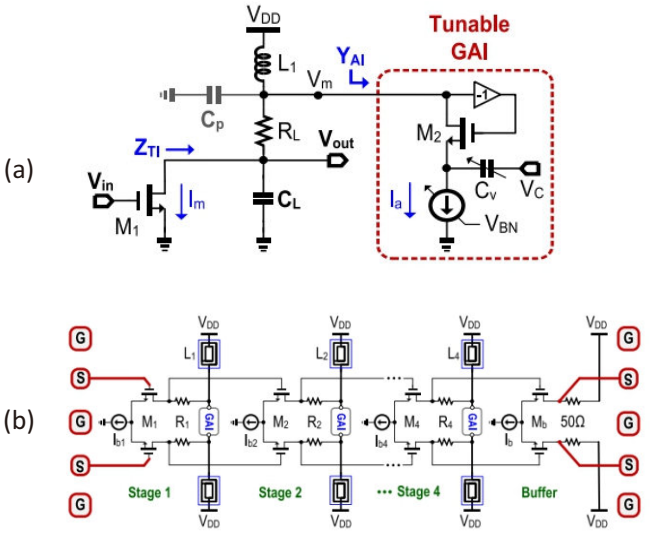
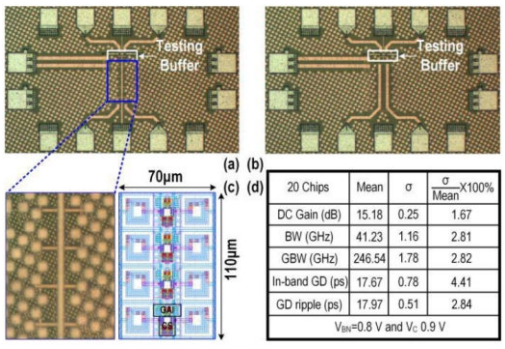


Fig. 1. (a) Simplified schematic of the proposed bridged-shunt peaking scheme with a tunable GAI. (b) Realized four-stage differential amplifier.



20 Chips	Mean	σ	$\frac{\sigma}{Mean}$X100%
DC Gain (dB)	15.18	0.25	1.67
BW (GHz)	41.23	1.16	2.81
GBW (GHz)	246.54	1.78	2.82
In-band GD (ps)	17.67	0.78	4.41
GD ripple (ps)	17.97	0.51	2.84
V_{BN}=0.8 V and V_C 0.9 V			

Fig. 2. (a) Amplifier's chip photograph. (b) Its reference path with an identical test buffer to de-embed the factual performances of the amplifier. (c) Layout details. (d) 20 chips were measured to confirm the robustness. [GBW = dc Gain × BW]

Publication(s)

[1] Y. Chen, P.-I. Mak, H. Yu, C. C. Boon, and R. P. Martins, "An Area-Efficient and Tunable Bandwidth-Extension Technique for a Wideband CMOS Amplifier Handling 50+ Gb/s Signaling," IEEE Transactions on Microwave Theory and Techniques, vol. 65, pp. 4960-4975, Dec. 2017.

Sponsorship

Research Committee of University of Macau (MYRG2017-00223-AMSV).

RESEARCH ABSTRACTS

High Resolution ADCs

A Low Supply Voltage Two-step TDC-assisted SAR ADC -------- 34

A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator With Multirate Opamp Sharing -------- 35

A 10-MHz Bandwidth Two-Path Third-Order ΣΔ Modulator with Cross-Coupling Branches -------- 36

A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance -------- 37

A 550µW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental ΣΔ ADC with 256 clock cycles in 65nm CMOS -------- 38

A Time-Interleaved 2nd-Order Δ Σ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation -------- 39

A Low Supply Voltage Two-step TDC-assisted SAR ADC

Minglei Zhang, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Supply = 0.6V

SNDR >70dB

Low power consumption, 82uW

SAR+TDC architecture

Silicon verified in 65 nm CMOS

DESCRIPTION

This paper presents a low power-supplied 13-bit 20-MS/s time-to-digital converter (TDC)-assisted successive approximation register (SAR) analog-to-digital converter (ADC). In this hybrid architecture, the voltage-to-time converter and TDC realizes inherent process, voltage, and temperature (PVT) robustness by inner tracking, thus inducing no extra power and circuit overheads. The voltage-domain and time-domain speed-enhanced techniques accelerate the 1st and 2nd stage ADC conversion under a low power supply, respectively. Furthermore, in cooperated with detect-and-skip switching scheme in the SAR ADC and offset bit shifting scheme in the two-step TDC, the ADC achieves a 13-bit linearity. The prototype ADC was fabricated in a 65-nm CMOS technology with a power supply of 0.6 V, achieving 71.0-dB signal-to-noise and distortion ratio (SNDR) and 89.5-dB spurious-free dynamic range with a Nyquist input at 20 MS/s, while with a Schreier figure-of-merit of 181.9 dB.

The prototype two-step TDC-assisted SAR ADC was fabricated in a 1P9M 65-nm CMOS process. Fig. 15 shows its die photograph with an active area of 0.053 mm2. The power supply and SAR ADC reference both have a voltage of 0.6 V. Large bypass capacitance is added on chip to stabilize the reference voltage, and the output data of the ADC is decimated by 5 to mitigate the ripple that couples through the PAD ring. The unit capacitors in the SAR ADC are custom designed encapsulated metal-oxide-metal capacitors. The ADC uses one-time on-chip foreground calibration for the offset and FS output time of the VTC, while the background bit shifting is applied to the TRG offset at off chip as introduced in Section IV-B. All the other error sources are covered by the redundancies between stages and the intrinsic matching.

The measured differential nonlinearity (DNL) and integral nonlinearity (INL) with a conversion rate of 20 MS/s. The measured DNL and INL errors are within −0.74/+0.72 LSB and −1.03/+1.31 LSB, respectively, benefiting from the high-linear CDAC in the SAR ADC. The measured 66 536-point fast Fourier transform (FFT) spectrums with both the LF and Nyquist input signals at 20 MS/s. The ADC achieves 71.5-dB SNDR and 91.9-dB spurious-free dynamic range (SFDR) with an input frequency of 0.49 MHz, and 71.0-dB SNDR and 89.5-dB SFDR with an input frequency of 9.98 MHz. The measured SNDR and SFDR versus various ADC input frequencies with a sampling rate of 20 MS/s. The SNDR and SFDR stay above 69.5 dB and 84.8 dB, respectively, even with an 18-MHz input signal.

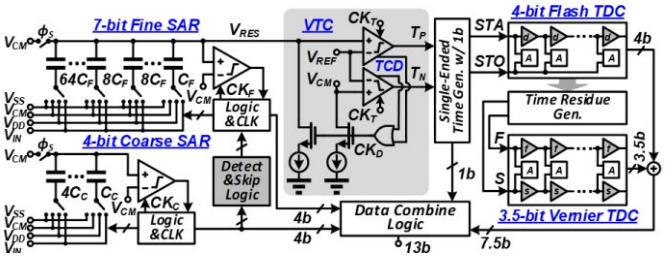


Fig. 1. Overall ADC Architecture and timing

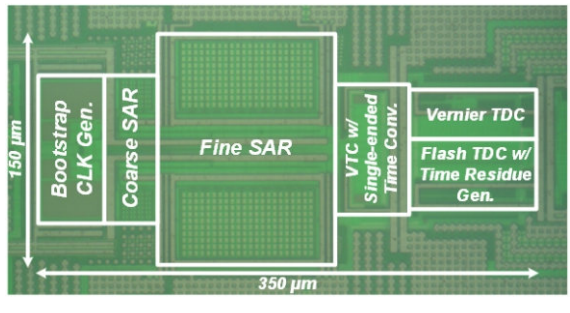


Fig. 2. Chip micrograph.

Publication(s)

[1] M. Zhang, C.-H. Chan, Y. Zhu, and R. P. Martins, “A 0.6V 13b 20MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed-enhanced techniques, in IEEE ISSCC Dig. Tech. Papers, Feb. 2019, pp. 66–67.

[2] M. Zhang, C. Chan, Y. Zhu and R. P. Martins, "A 0.6-V 13-bit 20-MS/s Two-Step TDC-Assisted SAR ADC With PVT Tracking and Speed-Enhanced Techniques," in IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3396-3409, Dec. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator With Multirate Opamp Sharing

Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti and R.P. Martins

FEATURES

Multirate Opamp Sharing Firstly Proposed in MASH

Op-amp sharing to improve the power efficiency

SAR utilized (offset insensitive)

Multi-rate mode at 120/240MHz

Silicon verified in 65 nm CMOS

DESCRIPTION

It is a DT 2-1 MASH Delta-Sigma modulator with multirate opamp sharing technique for ADC, targeting the optimization of power efficiency in active blocks, like opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-bit SAR quantizer and the DWA in the first stage enjoy additional operation time. Moreover, the stringent timing issue of the first quantizer and DWA caused by the horizontal sharing scheme was correctly addressed, thus allowing the incorporation of a SAR quantizer in the design. The use of a SAR is not only more power and area efficient, but free from the input-referred offset limitations of the quantizer.

Fabricated in 65-nm CMOS, this modulator runs at multirate 120/240MHz achieves a mean SNDR of 77.1dB for a 5MHz bandwidth, consuming 4.2mW from a 1.2V supply and occupying 0.066mm² core area. It exhibits a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB based on SNDR.

The measurement results show that this modulator achieved state-of-the-art performance. It enhances the opamps' power efficiency and the overall resolution further through allocating more reasonable settling time based on their various performance requests and capacitive loading. Therefore, we successfully exploit a high-resolution DT MASH at a signal bandwidth of 5MHz for LTE standards.

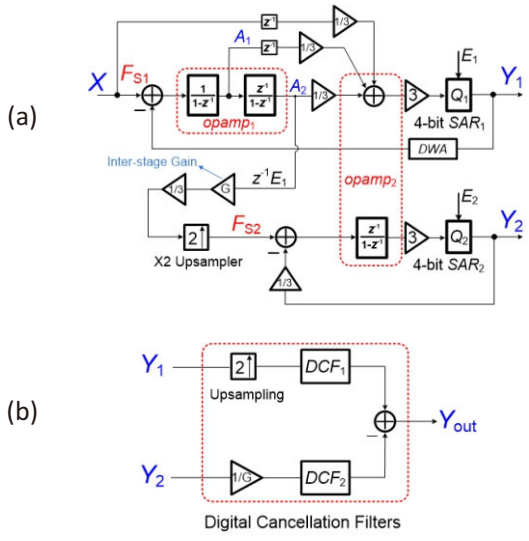


Fig. 1. (a) The proposed DT 2-1 MASH architecture and (b) its digital cancellation filters.

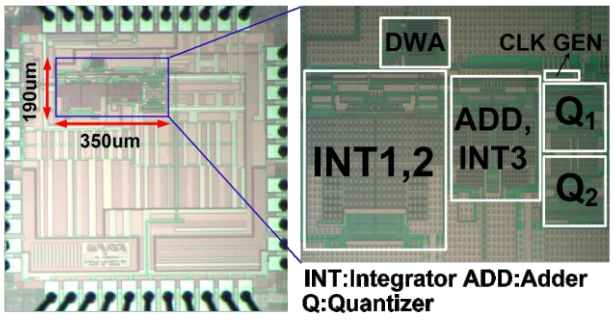


Fig. 2. Chip micrograph.

Publication(s)

[1] Liang Qi, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti, "A 12.5-ENOB 5MHz BW 4.2mW DT Multirate 2-1 MASH ΔΣ Modulator with Horizontal/Vertical Opamp Sharing in 65nm CMOS," ISSCC student research preview presentation, Feb. 2016.

[2] Liang Qi, Sai-Weng Sin, Seng-Pan U, Rui P. Martins, and Franco Maloberti, "A 4.2-mW 77.1-dB SNDR 5-MHz BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 64, no. 10, pp. 2641-2654, Oct. 2017.

Sponsorship

This work was supported by the Research Committee of University of Macau and Macao Science and Technology Development Fund(FDCT) under Grant FDCT/055/2012/A2.

A 10-MHz Bandwidth Two-Path Third-Order ΣΔ Modulator with Cross-Coupling Branches

Da Feng, Edoardo Bonizzoni, Franco Maloberti, Sai-Weng Sin and Rui Paulo Martins

FEATURES

Two-path architecture to reduce the channel speed

With an extra zero in modified NTF

Reduce the number of op-amps

Cross-coupling paths to realize the lowpass feature

Silicon verified in 65 nm CMOS

DESCRIPTION

It is a two-path discrete-time (DT) third-order sigma-delta (ΣΔ) modulator with an extra zero in the noise transfer function (NTF) located at z = −1, reducing the NTF coefficients of intermediate terms for optimal design. Applying polyphase decomposition of the NTF, the proposed ΣΔ modulator is implemented by a two-path architecture with cross-coupling branches.

This architecture optimizes the conventional 3rd-order modulator with a topological transformation of the basic scheme, by adding an extra zero in the NTF to reduce the intermediate terms. In addition, the extra zero ensures that applying the NTF polyphase decomposition technique, the proposed ΣΔ modulator can be implemented by a two-path architecture with cross-coupling branches, leading to performance at the state-of-the-art.

With cross-coupling branches, this modulator doubles the OSR for a given sampling frequency. The result is an increase of 3.5 bit in the resolution and a reduction of the power consumption. The techniques proposed in this brief allow using only two op-amps in each path at the cost of 1-bit of resolution.

The 65-nm CMOS experimental chip running at a sampling rate of 340 MHz achieves a DR of 68.8 dB and a SNDR of 65.4 dB for a 10-MHz signal bandwidth, occupying an active area of 0.2257 mm² and consuming 19.47 mW from a 1.2-V supply. The measured performance leads to a Walden FoM of 648.6 fJ/conversion-step and to a Schreier FoM of 152.4 dB (SNDR-based), respectively. With a lower FoMw and a smaller active area, the sampling frequency is about 40% higher than that of the conventional discrete-time implementations with the same CMOS technology.

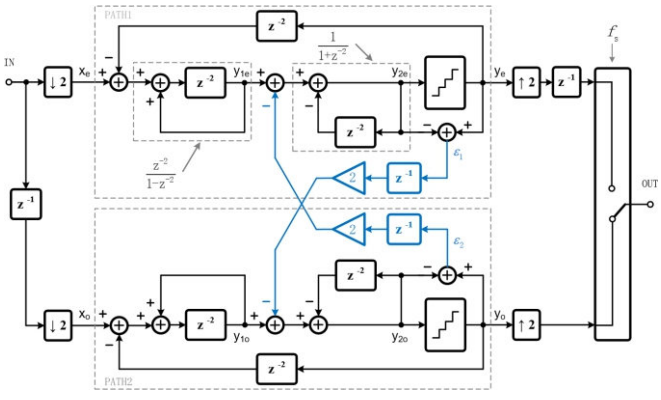


Fig. 1. Block diagram of the proposed third-order ΣΔ Modulator using a two-path architecture with cross-coupling branches.

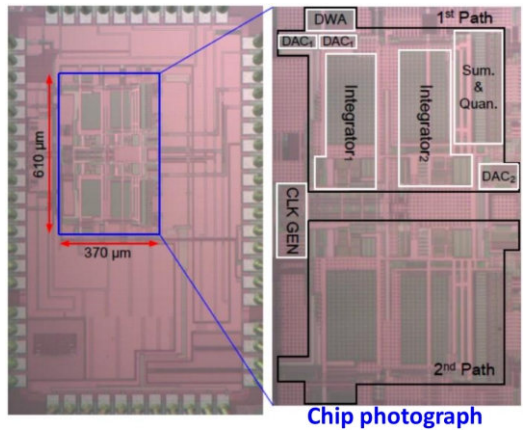


Fig. 2. Chip micrograph.

Publication(s)

[1] D. Feng, E. Bonizzoni, F. Maloberti, S. Sin and R. Martins, "A 10-MHz Bandwidth Two-Path Third-Order ΔΣ Modulator With Cross-Coupling Branches," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 10, pp. 1410-1414, Oct. 2018.

Sponsorship

This work was supported by Macau Science and Technology Development Fund (FDCT) under Grant FDCT/055/2012/A2.

A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance

Liang Qi, Ankesh Jain, Dongyang Jiang, Sai-Weng Sin, Seng-Pan U, Rui P. Martins and Maurits Ortmanns

FEATURES

Sturdy 3-0 MASH with wider bandwidth

Multibit DAC Nonlinearity Mitigation

NC works as dithering

Quantization Error Extraction in SAR

For 4G LTE-A Application

Silicon verified in 28 nm CMOS

DESCRIPTION

It is a dual-loop noise-coupling-assisted continuous time (CT) sturdy multi-stage noise shaping (SMASH) ΔΣ modulator (DSM), employing 1.5bit/4bit quantizers, respectively. The proposed SMASH can equivalently work as an overall fourth-order DSM with 4bit internal quantization.

To achieve 50MHz signal bandwidth for LTE-A applications, it is almost impossible to continue using a DT MASH architecture. Instead, a CT solution allows implementing such a large signal bandwidth. A CT sturdy MASH poses higher potential over a CT MASH owing to its relaxed matching requirement. Nevertheless, the quantization error cancellation and its extraction are still challenging in the CT domain.

On the other hand, DAC non-linearity becomes problematic with multi-GHz sampling frequency since DEM becomes less effective at low OSR while DAC calibrations often require large power and area consumptions.

A zeroth-order topology is intentionally selected for the second loop to accurately implement a unity-gain signal transfer function (STF) such that the 1.5bit noise leakage is minimized. Thereby, the proposed SMASH can equivalently work as an overall fourth-order DSM with 4bit quantization. The noise coupling applied in the SMASH whitens 1.5bit quantization noise and further reduces its in-band tone power, while a finite impulse response (FIR) filter integrated into the outermost feedback path suppresses the out-of-band noise power of the DAC input. Together, this circumvents any linearization technique for multibit DACs.

Fabricated in 28nm CMOS technology, this prototype measures an SNDR of 76.6dB and an SFDR of 87.9dB over a 50MHz bandwidth, consuming 29.2mW from 1.2V/1.5V supplies and occupying an active area of 0.085mm². It exhibits a Schreier figure-of-merit (SNDR) of 168.9dB.

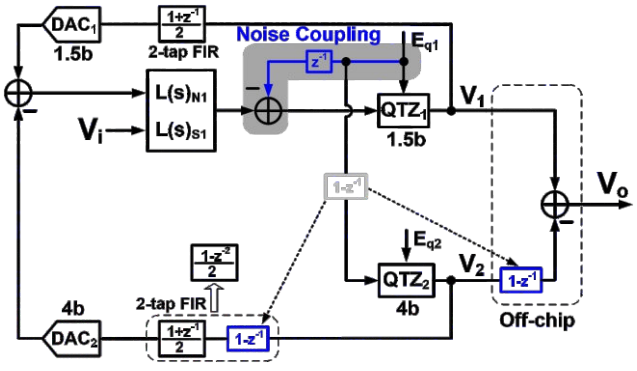


Fig. 1. Block diagram of the proposed CT dual-loop SMASH

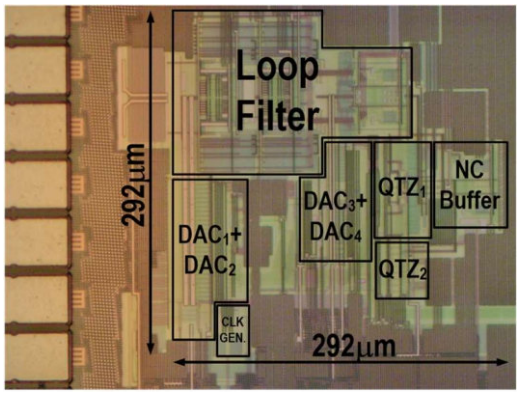


Fig. 2. Chip micrograph.

Publication(s)

[1] L. Qi, A. Jain, D. Jiang, S. Sin, R. P. Martins and M. Ortmanns, "20.5 A 76.6dB-SNDR 50MHz-BW 29.2mW Noise-Coupling-Assisted CT Sturdy MASH ΔΣ Modulator with 1.5b/4b Quantizers in 28nm CMOS," 2019 IEEE International Solid-State Circuits Conference - (ISSCC), 2019, pp. 336-338.

[2] L. Qi, A. Jain, D. Jiang, S. Sin, R. P. Martins and M. Ortmanns, "A 76.6-dB-SNDR 50-MHz-BW 29.2-mW Multi-Bit CT Sturdy MASH With DAC Non-Linearity Tolerance," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 344-355, Feb. 2020

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was funded by the Science and Technology Development Fund, Macau SAR (File no.076/2017/A2 & SKL-AMSV-2017-2019(DP)).

A 550µW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental ΣΔ ADC with 256 clock cycles in 65nm CMOS

Biao Wang, Sai-Weng Sin, Seng-Pan U, Franco Maloberti and R.P. Martins

FEATURES

First Linear-Exponential IADC

Linear-phase: lower KT/C penalty factor

Exponential-phase: Boosting the SQNR

Noise-coupling technique

Silicon verified in 65 nm CMOS

DESCRIPTION

It is an incremental analog-to-digital converter (IADC) with a two-phase linear-exponential accumulation loop. In the linear phase, the loop works as a first-order structure. The noise-coupling path is then enabled in the exponential phase thus boosting the SQNR exponentially with a few numbers of clock cycles.

The two-phase scheme combines the advantages of the thermal noise suppression in the 1st order IADC and SQNR boosting in the exponential mode. The uniform-exponential weight function allows the data weighted averaging (DWA) technique to work well, leading to the rotation of the multi-bit DAC mismatch error. Meanwhile, this scheme does not destroy the notches, which can be utilized to suppress the line noise.

In the initial 246 cycles of the linear phase, the IADC works as a 1st-order architecture and fully utilizes the oversampling operation on thermal noise suppression. After that, the circuit reconfigured as an exponential phase, boosts the SQNR exponentially in 10 clock cycles. It achieved the exponential accumulation with the noise-coupling ping-pong SC circuit. The uniform-exponential weighting allows the DWA technique to work well in improving the linearity by rotating the multi-bit DAC elements.

The prototype IADC that has been implemented in a 1P7M 65nm CMOS process, occupying an active area of 0.134 mm². With 1.2V supply, the ADC reaches an SNDR/DR of 100.8dB/101.8dB with 20kHz BW while consuming 550µW, resulting in an Walden/Schreier FoMW/FoMS of 153fJ /176.4dB, respectively. The DWA technique produces high linearity with DNL/INL of 0.27/0.84 LSBs.

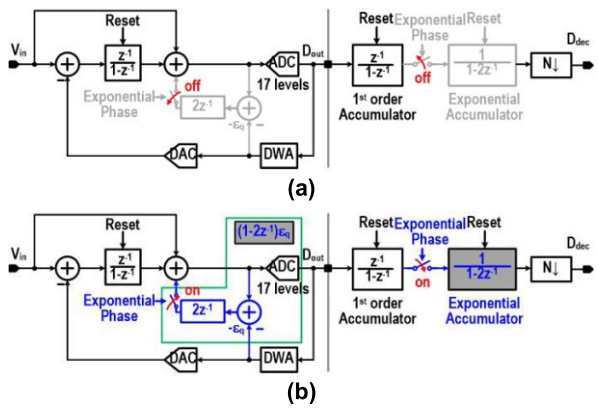


Fig. 1. Block diagram of the proposed Incremental ADC at (a) Linear-Phase and (b) Exponential-Phase.

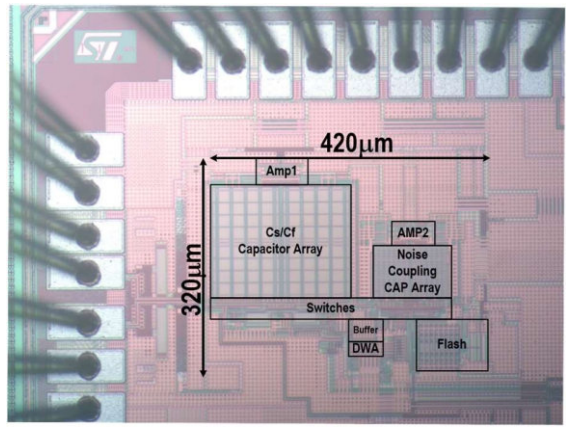


Fig. 2. Chip micrograph.

Publication(s)

[1] B. Wang, S. Sin, U. Seng-Pan, F. Maloberti and R. P. Martins, "A 550µW 20kHz BW 100.8DB SNDR Linear-Exponential Multi-Bit Incremental Converter with 256-cycles in 65NM CMOS," 2018 IEEE Symposium on VLSI Circuits, 2018, pp. 207-208.

[2] B. Wang, S. Sin, S. U., F. Maloberti and R. P. Martins, "A 550-µW 20-kHz BW 100.8-dB SNDR Linear- Exponential Multi-Bit Incremental ΔΣ ADC With 256 Clock Cycles in 65-nm CMOS," in IEEE Journal of Solid-State Circuits, vol. 54, no. 4, pp. 1161-1172, April 2019. (Invited Special Issue of VLSI).

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was supported in part by Science and Technology Development Fund, Macau under Grant 055/2012/A2 and in part by the Research Committee of University of Macau under Grant MYRG2017-00192-FST.

A Time-Interleaved 2nd-Order Δ Σ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation

Dongyang Jiang, Liang Qi, Sai-Weng Sin, Franco Maloberti and R.P. Martins

FEATURES

Digital-feedforward extrapolating TI ΔΣM
Quadrable OSR = 208
Full-extrapolation in digital domain
Dithering to enhance the linearity
Silicon verified in 28 nm CMOS

DESCRIPTION

It presents a 4x time-interleaved (TI) 2nd-order discrete-time (DT) delta-sigma modulator (DSM). We propose a digital feed-forward extrapolation by first digitizing the internal analog nodes' information from one channel, and then extrapolating the other channels in the digital domain. As a result, this DSM only needs two operational amplifiers (op-amps) to realize four interleaving paths, thus reducing analog hardware overheads.

The digital feedforward extrapolation works by firstly digitizing the essential analog nodes' information (i.e., X, P_1, and P_2) from one channel and then fully extrapolating the other channels in the digital domain. This operation not only removes all burden analog adders, but also bypasses stringent matching requirements between the analog/digital extrapolating gains. Meanwhile, we linearize the digital feed-forward paths through injected dithering.

Fabricated in 28nm CMOS technology, the channel's clock is 520 MS/s, which leads to an equivalent sampling rate of 2.08GS/s. the increased sampling frequency results in two possible directions: 1) increase the OSR but with a fixed BW or 2) increase the BW with a fixed OSR. This implementation is the latter case, such ADC increased the effective output OSR from 52 to 208 with the BW fixed at 5MHz. The achieved peak SNDR is 86.1-dB. The ADC consumes a total of 23.1-mW with 1/1.15/1.5V power supplies, which results in a Schreier Figure of Merit (FOM) (based on SNDR) of 169.5dB.

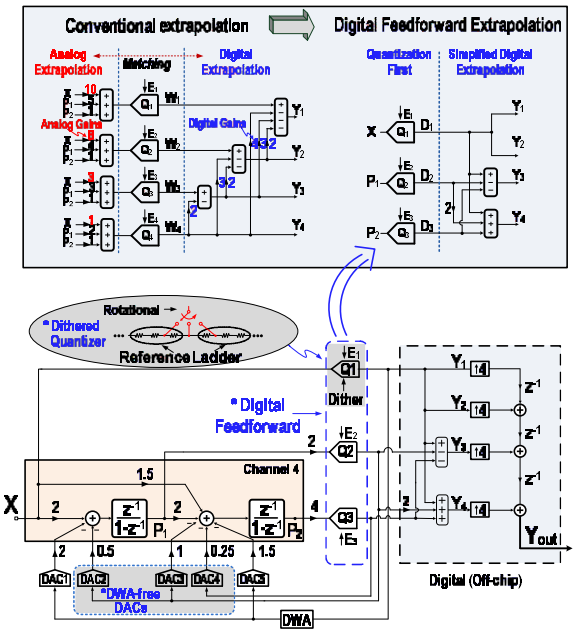


Fig. 1. System-level architecture of the extrapolating TI DSM (top) with conventional/ digital feedforward extrapolation comparison (bottom.)

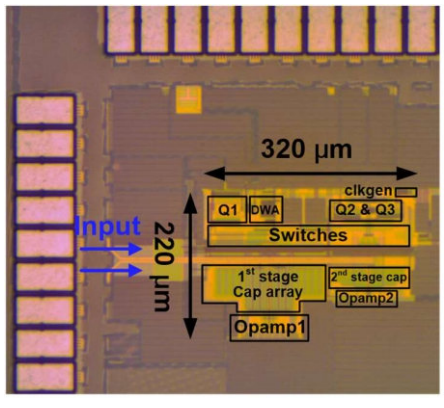


Fig. 2. Chip micrograph.

Publication(s)

[1] D. Jiang, L. Qi, S. -W. Sin, F. Maloberti and R. P. Martins, "A 5MHz-BW, 86.1dB-SNDR 4X Time-Interleaved 2nd-Order ΔΣ Modulator with Digital Feedforward Extrapolation in 28nm CMOS," 2020 IEEE Symposium on VLSI Circuits, 2020, pp. 1-2

[2] D. Jiang, L. Qi, S. -W. Sin, F. Maloberti and R. P. Martins, "A Time-Interleaved 2nd-Order Δ Σ Modulator Achieving 5-MHz Bandwidth and 86.1-dB SNDR Using Digital Feed-Forward Extrapolation," in IEEE Journal of Solid-State Circuits, 2021, in early access.

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was funded by The Science and Technology Development Fund, Macau SAR [File no. 076/2017/A2, SKL-AMSV(UM)-2020-2022], and The Ministry of Science and Technology, China. [File no. EF001/AMSV/2018/MOST].

RESEARCH ABSTRACTS

High Speed ADCs

A Wideband Continuous-time Sigma Delta Modulator -------- 41

A Wideband Dynamic Amplifier Reused NS Pipeline-SAR ADC -------- 42

A 14-bit Split-Pipeline ADC with Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current -------- 43

LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter with Ripple Calibration -------- 44

A Wideband Noise-Shaping Pipeline-SAR ADC -------- 45

A Wideband Continuous-time Sigma Delta Modulator

Wei Wang, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Bandwidth > 100MHz

Continuous-time sigma delta modulator

Low power consumption, 16.3mW

Preliminary sample and quantization technique

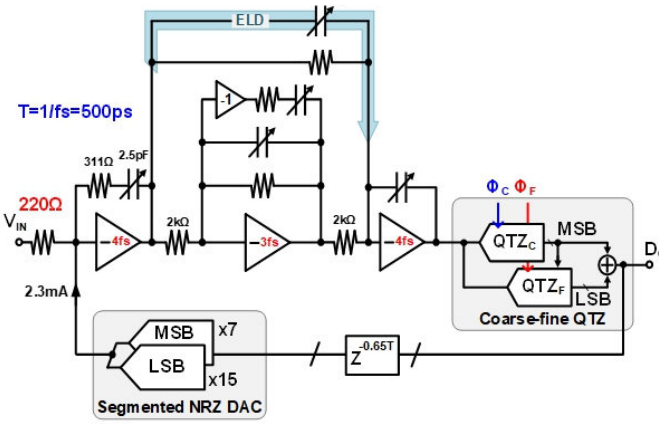
SAR ADC as quantizer

Silicon verified in 28 nm CMOS

DESCRIPTION

This paper reports a 4th-order 100 MHz bandwidth continuous-time (CT) delta-sigma modulator in 28 nm CMOS. A preliminary sampling and quantization (PSQ) technique is presented, which allows almost a full utilization of the clock period for the quantization to extend the available conversion time of the backend quantizer under a 0.65 ELD coefficient. With the PSQ, both the sampling and quantization of the backend quantizer are split into 2-step, coarse and fine, similar to the subranging architecture to save power. The quantizer runs at 2 GHz achieving 7-bit (1b error correction) with only 1.4 mW power. By adding a feedforward ELD compensation path in the cascade of integrators of the CIFF topology, only one DAC is necessary in this design. The modulator attains a signal bandwidth of 100 MHz with 72.6 dB SNDR while only consuming 16.3 mW from 1.1 V and 1.5 V power supplies. The prototype has a dynamic range of 76.3 dB and a Schreier FoM of 174.2 dB with an active area of 0.019 mm^2.

The CT ΔΣ modulator is realized in 28 nm CMOS has an active area of 0.19 mm^2. The power supply of the QTZ is 1.1V and the NRZ DAC is with 1.5V supply for the low noise considerations. The other parts are working under a 1V supply. The sampling frequency of the modulator is 2 GHz with 10 OSR. The 0.65Ts ELD and 0.25Ts are realized by inverters' delay which vary under PVT. In this design, we make only the fine sampling instant tunable for the best speed performance. The bandwidth is 100MHz. The output spectrum of the modulator with a -2 dBFS, 1.4Vpp single-tone signal at ~18 MHz input frequency. The SNDR, SNR and spurious-free dynamic range (SFDR) are 72.6 dB, 73.2 dB and 83.6 dB, respectively after the DAC mismatch calibration. The 80 dB/decade spectral slope validates the 4th-order noise shaping realized by the SAB and two conventional integrators.



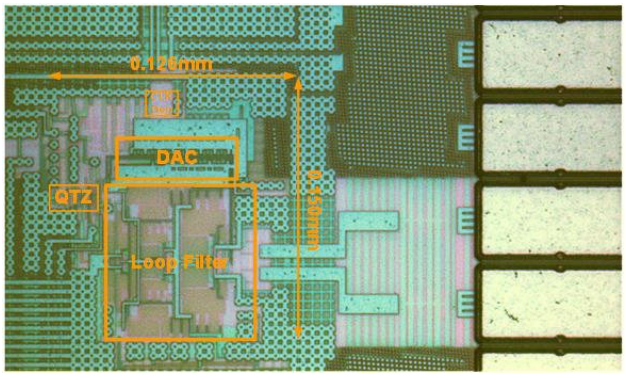


Fig. 2. Chip micrograph.

Publication(s)

[1] W. Wang, C. Chan, Y. Zhu and R. P. Martins, "20.7 A 72.6dB-SNDR 100MHz-BW 16.36mW CTDSM with Preliminary Sampling and Quantization Scheme in Backend Subranging QTZ," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 340-342.

[2] W. Wang, C. Chan, Y. Zhu and R. P. Martins, "A 100-MHz BW 72.6-dB-SNDR CT ΔΣ Modulator Utilizing Preliminary Sampling and Quantization," in IEEE Journal of Solid-State Circuits, vol. 55, no. 6, pp. 1588-1598, June 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT),Research Committee of University of Macau.

A Wideband Dynamic Amplifier Reused NS Pipeline-SAR ADC

Yan Song, Yan Zhu, Chi-Hang Chan and Rui P. Martins

FEATURES

Bandwidth > 40MHz

Noise-Shaping Pipeline-SAR

Low power consumption, 2.56mW

Flip around error feedback Noise-shaping

Dynamic amplifier reused

Silicon verified in 28 nm CMOS

DESCRIPTION

This article presents a successive approximation register (SAR)-assisted noise-shaping (NS) pipeline analog-to-digital converter (ADC) incorporating various techniques to improve its bandwidth (BW), energy efficiency as well as robustness. A multiple-input dynamic amplifier is utilized for both residue amplification and error feedback (EF) summation, thus realizing a 1st-order NS with low power consumption. An additional residue feed-forward (FF) path is introduced in the 2nd stage SAR ADC to compensate for the NTF deterioration caused by the gain mismatch in the multiple-input pairs of the dynamic amplifier. The partial interleaving 1st stage breaks the speed bottleneck of conventional 3-phase timing arrangement, which significantly enhances the overall ADC's speed and sampling performance. Besides, a coarse SAR ADC is introduced to further speed up the conversion with low power, while simultaneously enabling the enclosure of the data-weighted-averaging (DWA) on the DAC without a speed penalty. Finally, a low-cost inter-stage offset calibration is proposed that aligns the offset voltages among stages in the background without requiring an extra phase.

The ADC prototype fabricated in 28-nm CMOS process occupies an active area of 0.016mm^2.The pseudo-random noise generator, DWA, and inter-stage offset calibration logic account for only 1%, 1.3%, 1% of the total ADC's area, respectively. The ADC operates at the sampling rate of 600 MHz and achieves a BW up to 40 MHz at an OSR = 7.5. The measured FFT spectrum when the DWA is disabled. The actual pole of the NTF in this sample is estimated to be 0.6, which is affected by the mismatch variations, as discussed in Section III B. Under such condition, the FF NS path can still contribute an extra 4-dB SQNR which compensates the NTF deterioration originated from the α variation. The measured 32768-point FFT spectrum with a 2 MHz, -0.4 dBFS sinusoidal input signal at different calibration configurations. With all calibrations enabled, the prototype reaches a peak SNDR and spurious-free-dynamic-range (SFDR) of 75.2 dB and 87.1 dB, respectively. The residual DAC mismatches and the non-linearity from the dynamic amplifier impose the remaining harmonics.

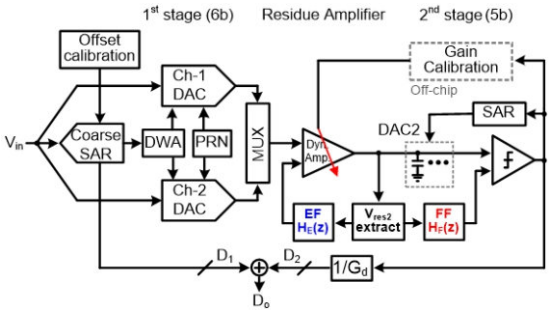


Fig. 1. Overall ADC Architecture and timing

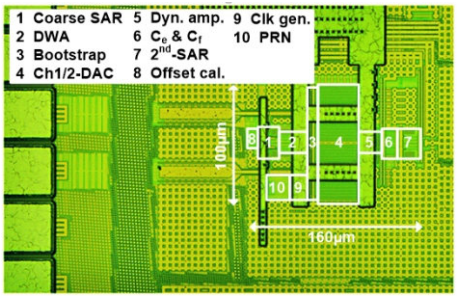


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Song, Y. Zhu, C. H. Chan and R. P. Martins, "9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 164-166.

[2] Y. Song, Y. Zhu, C. -H. Chan and R. P. Martins, "A 40-MHz Bandwidth 75-dB SNDR Partial-Interleaving SAR-Assisted Noise -Shaping Pipeline ADC," in IEEE Journal of Solid-State Circuits, vol. 56, no. 6, pp. 1772-1783, June 2021

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 14-bit Split-Pipeline ADC with Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current

Jiaji Mao, Mingqiang Guo, Sai-Weng Sin, and Rui P. Martins

FEATURES

High-speed: 100MS/s Sampling Rate

High-resolution: 14-bit

Low power consumption: Optimizes duty-cycle ratio

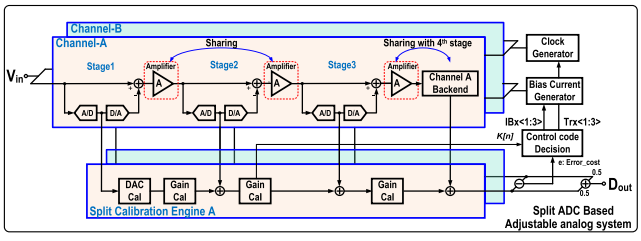
Background Calibration: Inter-stage gain (that includes settling) error

Silicon verified in 65 nm CMOS

DESCRIPTION

It presents a 14-bit split-pipeline opamp-sharing ADC, with background calibration that optimizes duty-cycle ratio and amplifier power consumption in the sharedopamp. Based on the interstage gain (that includes settling) error estimated by the split ADC calibration engine, the clock duty-cycle ratio and the bias current are adjusted to achieve better dynamic settling and resolution trade-offs.

Operating at 100MS/s with a 9-MHz input signal, the ADC achieves 46.5dB of Signal-to-Noise-and-Distortion Ratio (SNDR), and 59.6dB of Spurious-Free Dynamic Range (SFDR) before calibration, and after calibration, it improves to 71.7dB of SNDR and 84.4dB of SFDR, respectively. The ADC maintains an SNDR over 68.5dB within the full Nyquist bandwidth consuming 32mW of power, which yields a Walden Figure-of-Merit (FoM) of 147.2 fJ/conversion-step and a Schreier FoM of 160.4dB.



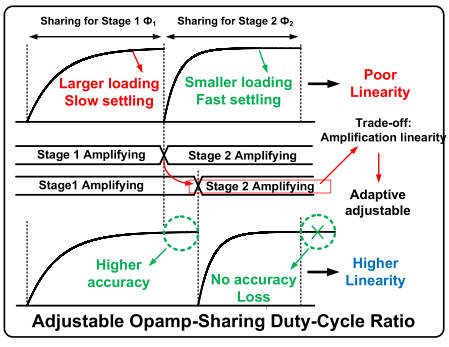


Fig. 1. The architecture split-pipeline ADC with self-adjustable opamp-sharing duty-cycle ratio.

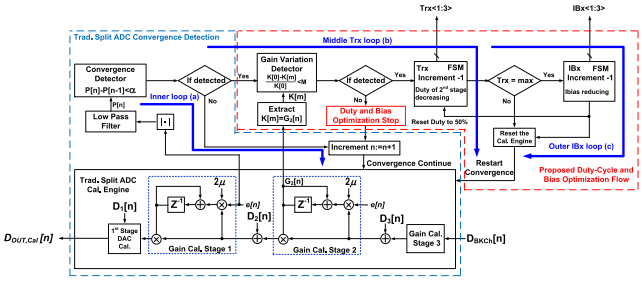


Fig. 2. The flow chart of the calibration algorithm.

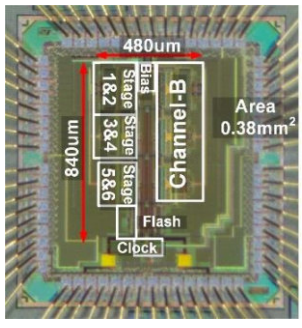


Fig. 3. Block diagram and chip micrograph of 7/8-way split TI ADC.

Publication(s)

[1] J. Mao, M. Guo, S. Sin and R. P. Martins, "A 14 bit Split Pipeline ADC with self-adjusted opamp-sharing duty cycle," IEEE ISSCC Student Research Preview, Feb. 2018.

[2] J. Mao, M. Guo, S. Sin and R. P. Martins, "A 14-Bit Split-Pipeline ADC With Self-Adjusted Opamp-Sharing Duty-Cycle and Bias Current," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 10, pp. 1380-1384, Oct. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT, File no. 055/2012/A2), Research Committee of University of Macau (File no.: MYRG2017-00192-FST).

LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter with Ripple Calibration

Hanyu Wang, Sai-Weng Sin, Chi-Seng Lam, Franco Maloberti and R.P. Martins

FEATURES

First integrates on-chip DC-DC converter with the ADC, without the use of any LDOs

On-chip Boost DC-DC (power efficiency of 78.6%)

10-bit 500MS/s pipelined ADC

Ripple calibration technique

Silicon verified in 65 nm CMOS

DESCRIPTION

It presents a compact power management solution for a pipeline ADC, employing only a switching-mode power converter. By directly powering the ADC using a boost DC-DC converter, the power delivery network (PDN) exhibits an overall-high power efficiency. The proposed foreground ADC calibration calibrates the ripple error induced from the power converter, which obviates the need for well-regulated supply and reference voltage offered by low-efficiency linear low-dropout regulators (LDOs).

This chip integrates the boost DC-DC converter and the pipelined ADC with an external power inductor. Due to the periodic switching operation, the voltage ripple from the DC-DC converter is also periodic, which makes it feasible to sense and calibrate such errors. Nevertheless, ADC with rippled reference is unable to detect the ripple voltage directly. Thus, the backend ADC demands a clean DC reference source. This work reconfigures the ADC's first stage to a ripple-free sample-and-hold amplifier with a gain of four in the calibrating phase to generate a DC voltage V_CAL for backend ADC, finally implements a clean calibration reference in the foreground to achieve the ripple calibration purpose.

This 65-nm CMOS prototype occupies 2.34-mm² of total active area (9.4%-ADC, 2.6%-power controller and switches, and 88%-output capacitance). In the measurement, the boost converter, switching at 31.25MHz, converts a 0.5V input to 1.2V and delivers 22.8mW of power to the pipeline ADC. The boost DC-DC converter supplies all voltage domains, including analog/digital power supply and reference. The resulting overall system power efficiency is 78.6%. Sampled at 500MS/s, the ADC achieves a signal-to-noise and distortion ratio (SNDR) of 34.7/39.9dB without/with the ripple calibration for an input frequency of 177MHz, respectively.

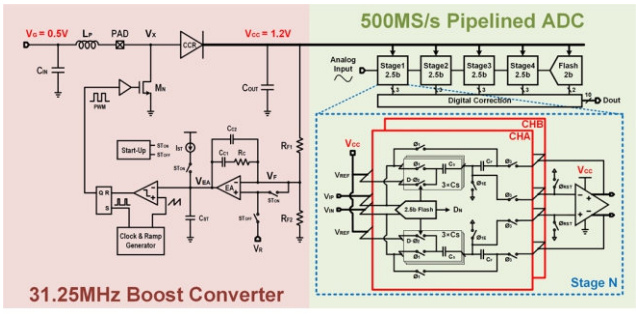


Fig. 1. Overview of the system architecture: the boost converter directly powers all pipelined ADC voltage domains, including power supply and reference voltage.

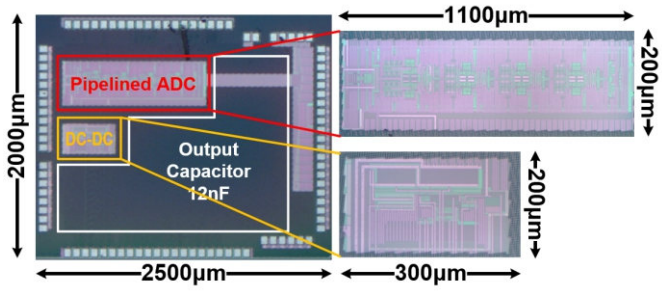


Fig. 2. Chip micrograph.

Publication(s)

[1] H. Wang, S. -W. Sin, C. -S. Lam, F. Maloberti and R. P. Martins, "LDO-Free Power Management System: A 10-bit Pipelined ADC Directly Powered by Inductor-Based Boost Converter With Ripple Calibration," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 12, pp. 4174-4186, Dec. 2020.

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was supported in part by the Science and Technology Development Fund, Macau SAR, under Grant SKL-AMSV(UM)-2020-2022 and Grant SKL-AMSV-ADDITIONAL FUND and in part by the Research Committee of University of Macau under Grant MYRG2017-00192-FST.

A Wideband Noise-Shaping Pipeline-SAR ADC

Yan Song, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Bandwidth > 12.5MHz
Noise-Shaping Pipeline-SAR
Low power consumption, 4.5mW
Flip around error feedback Noise-shaping
Opamp reused
Silicon verified in 65 nm CMOS

DESCRIPTION

This paper presents a successive approximation register (SAR)-assisted noise-shaping (NS) pipeline architecture which breaks the speed bottleneck of existing SAR or SAR-assisted type NS analog-to-digital converters (ADCs). Rather than only for residue amplification and pipeline operation, the multiplying digital-to-analog converter (MDAC) is also reused as unity buffer and analog adder to realize the NS with error feedback (EF) structure in this design. While incorporating the proposed alternative loading capacitor (ALC) technique, an ideal 1st-order noise transfer function (NTF) is realized without additional feedback phase and only with a small analog circuit overhead. Unlike other NS SAR ADCs that involved amplification, the inter-stage gain attenuates the noise from the 2nd-stage comparator, thus leading to both high speed and resolution. Fabricated in 65 nm CMOS process, the prototype achieves a signal-to-noise-and-distortion ratio (SNDR) of 77.1 dB over 12.5 MHz BW with only 8 over–sampling ratio (OSR). Under a 1.2 V supply voltage, the ADC consumes 4.5 mW and exhibits a Scherier figure-of-merit (FoMs) of 171.5 dB.

The chip micro-photograph of the ADC prototype fabricates in 65nm CMOS with an active area of 0.014 mm2. The ADC has a BW that goes up to 12.5 MHz with 200 MS/s and OSR = 8. The FFT spectrum with a 1.5 MHz, −0.75dBFS sinusoidal input signal, with the prototype reaching the peak SNDR and a spurious-free-dynamic-range (SFDR) of 77.1 dB and 90.7 dB, respectively. The capacitor mismatch in the 1st-stage DAC is foreground calibrated by estimating the actual DAC bit-weight based on the least-mean-square (LMS) algorithm. The remaining harmonics appear in the spectrum due to the sampling and calibration accuracy limitations. Under a supply voltage of 1.2 V, the ADC consumes 4.5 mW and results in a FoMs of 171.5 dB. We measured 6 samples with the same testing setup, which confirm that they have a stable SNR and SNDR with only a small variation range less than 1 dB. The measured SNR and SNDR versus input amplitude, showing that the dynamic range (DR) is 78.5 dB. The measured SNR and SNDR versus OSR. Due to the noise floor, the SNR increases about 7 dB when the OSR doubles (with small OSRs), thus indicating a 1st-order NTF in our prototype.

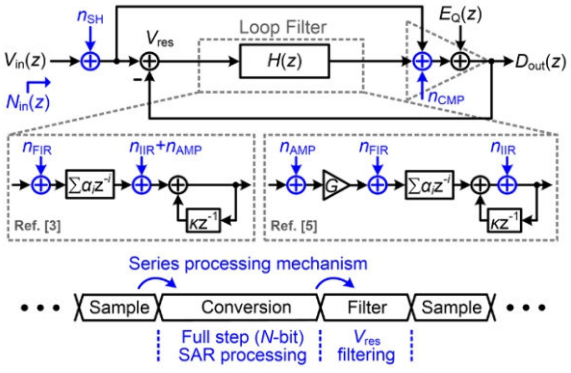


Fig. 1. Overall ADC Architecture and timing.

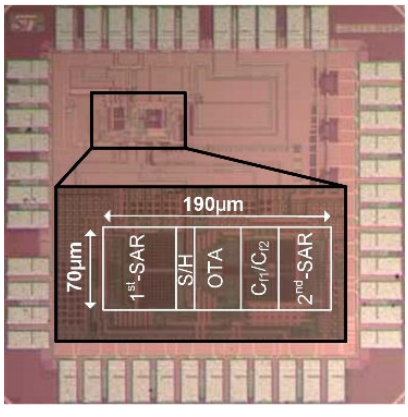


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Song, Y. Zhu, C. Chan, L. Geng and R. P. Martins, "A 77dB SNDR 12.5MHz Bandwidth 0–1 MASH ∑Δ ADC Based on the Pipelined-SAR Structure," 2018 IEEE Symposium on VLSI Circuits, 2018, pp. 203-204.

[2] Y. Song, C. Chan, Y. Zhu and R. P. Martins, "A 12.5-MHz Bandwidth 77-dB SNDR SAR-Assisted Noise Shaping Pipeline ADC," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 312-321, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

RESEARCH ABSTRACTS

Sub-GHz to GHz ADCs

A GHz Sampling Rate Multi-bit PVT Robust SAR ADC -------- 47

A High-speed TDC-based ADC -------- 48

A Single Channel GHz Sampling Rate Fully Dynamic Pipeline ADC -------- 49

A 1.6GS/s 12.2mW 7/8-way Split Time-Interleaved SAR ADC achieving 54.2-dB SNDR with Digital Background Timing Mismatch Calibration -------- 50

A 5 GS/s 29 mW Interleaved SAR ADC Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications -------- 51

A 3-stage GHz Sampling Rate Fully Dynamic Pipeline ADC -------- 52

A GHz Sampling Rate Multi-bit PVT Robust SAR ADC

Chi-Hang Chan, Yan Zhu, Wai-Hong Zhang, Seng-Pan U and Rui P. Martins

FEATURES

Sampling Rate > 2.4Hz
Low power consumption, 5mW
Lowe input capacitance, 64fF
Background offset calibration
Stable SNDR up to Nyquist input
Silicon verified in 28 nm CMOS

DESCRIPTION

This paper presents a 2x time-interleaved 7-bit 2.4 GS/s 1-then-2b/cycle SAR ADC in 28nm CMOS. The Process-Voltage-Temperature (PVT) sensitivity of a multi-bit SAR architecture has been improved by the proposed 1-then-2b/cycle scheme with background offset calibration. With the Pre-charge Reduction Scheme (PRS), the traditional large switching energy and time consuming pre-charge operation have been removed, which simultaneously enables a simple control logic without the need of a Vcm voltage. Besides, a background offset calibration is implemented on-chip which does not involve any which does not involve any extra phase or calibration input signal. Its operation is well embedded within the 1-then-2b/cycle architecture, thus leading to a very minimal modification of the ADC core. With an improved fringing DAC structure and a high-speed dynamic logic circuit, a single channel ADC can work at 1.2 GS/s under a 0.9V supply. Using two ways time-interleaving, the prototype samples at 2.4 GHz and consumes 5 mW power including the on-chip background offset calibration.

The ADC realized in a 28 nm 1P9M CMOS process. The active area is 0.043 mm² including the on-chip background offset calibration. The input capacitance is around 64 fF including parasitics but without considering the input routing, PAD and ESD devices. The SNDR under a wide range of temperature, supply and common-mode voltage variations with low frequency input. The chip with worst performance is #3 while it is still able to keep a SNDR above 35 dB from -40 to 125℃. When running at around 2 GS/s, the SNDR of the chip #3 stays above 38 dB in a ±10% supply and common-mode voltage variations. Comparing this work with the state-of-the-art ADCs, it achieves a good energy efficiency with the necessary calibration on-chip.

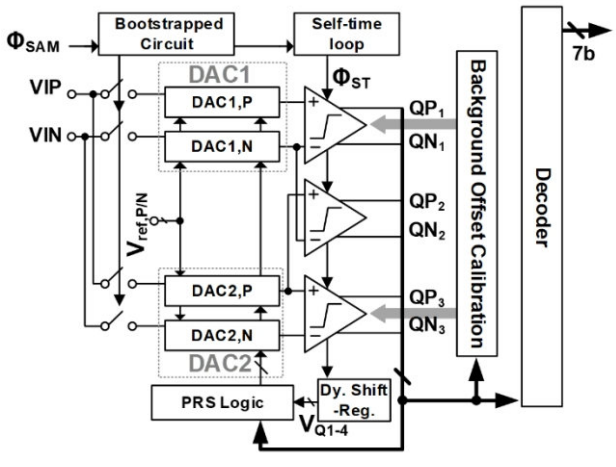


Fig. 1. Overall ADC Architecture.

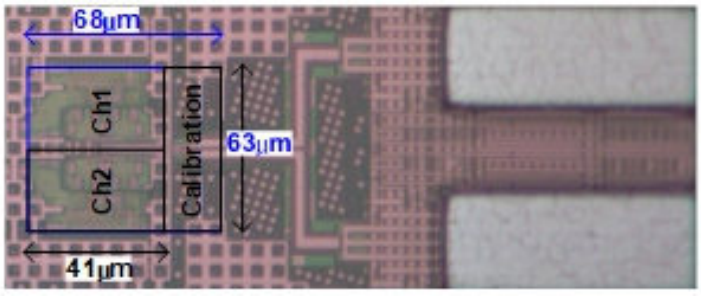


Fig. 2. Chip micrograph.

Publication(s)

[1] C. H. Chan, Y. Zhu, I. M. Ho, W. H. Zhang, S. P. U and R. P. Martins, “A 5mW 7b 2.4GS/s 1-then-2b/cycle SAR ADC with background offset calibration, ” in International Solid-State Circuits Conference (ISSCC) Dig. Tech. Papers, pp. 282-283, Feb. 2017.

[2] C. Chan, Y. Zhu, W. Zhang, S. U and R. P. Martins, "A Two-Way Interleaved 7-b 2.4-GS/s 1-Then-2 b/Cycle SAR ADC With Background Offset Calibration," in IEEE Journal of Solid-State Circuits, vol. 53, no. 3, pp. 850-860, March 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A High-speed TDC-based ADC

Minglei Zhang, Yan Zhu, Chi-Hang Chan and Rui P. Martins

FEATURES

Sampling rate > 10GHz
TDC-ADC
Low power consumption, <50mW
On-chip calibration and low BER
Large ERBW
Silicon verified in 65 nm CMOS

DESCRIPTION

This paper presents an 8-bit time-domain analog-to-digital converter (ADC) that achieves 10 GS/s by aggregating only four time-interleaved channels. It also experiences less than 3.0-dB signal-to-noise and distortion ratio (SNDR) drop at an 18-GHz input frequency from a DC input due to its small input capacitance and inherent voltage-to-time converter (VTC)-based sub-channel buffer. A 16× time interpolation-based time-to-digital converter (TDC) resolves in two steps while allows both the inter-stage gain and the quantization step to be free from calibration over PVT variations. Furthermore, through a timing-extended residue transfer scheme, the metastability error rate is suppressed to <10-8. Fabricated in a 65-nm CMOS process, the prototype ADC achieves a 40.1-dB SNDR for a Nyquist input signal at 10 GS/s while consuming 50.8 mW from a 1.0-V power supply, yielding a Walden figure-of-merit of 61.5 fJ/conversion-step.

The prototype 8-bit 10-GS/s time-domain ADC was fabricated in a 1P9M 65-nm CMOS process. The chip die micrograph with an active area of 0.095 mm2. The chip die is bonded on a printed circuit board with <0.5-mm critical bonding wires. High-speed ADC measurement strategy with input amplitude and phase monitor is adopted in this work. The ADC has a power supply of 1.0 V with separated supply domains for different blocks and a large decoupling capacitance to reduce the crosstalk among supplies. For the most critical situation where all blocks share the same supply trace with 1-nH bonding wire and 200-pF decoupling capacitance, simulation results show that the ADC SNDRs reduces from 52.3 dB to 48.9 dB and 45.6 dB at the LF and Nyquist inputs, respectively, excluding the noise and random quantization mismatch. One-time foreground calibration is applied to remove the offset of VTCs for better dynamic range performance. The gain, remaining offset, and time skew between different channels are removed in the background together with the residue transfer offset, while the calibration is enabled occasionally to track the slow drift of the ambient temperature and supply voltage. No calibration related to the time quantization steps and inter-stage gain is applied, benefiting from the 16× interpolation-based two-stage architecture.

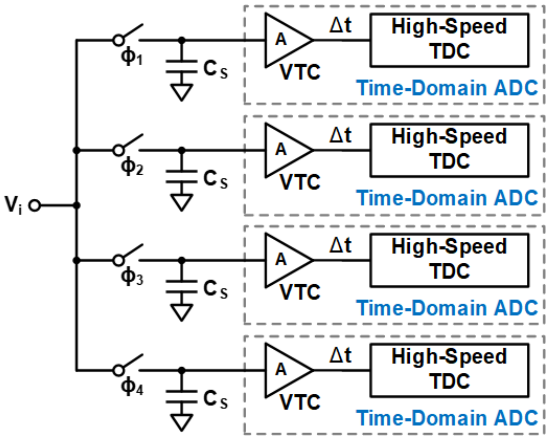


Fig. 1. Overall ADC Architecture and timing

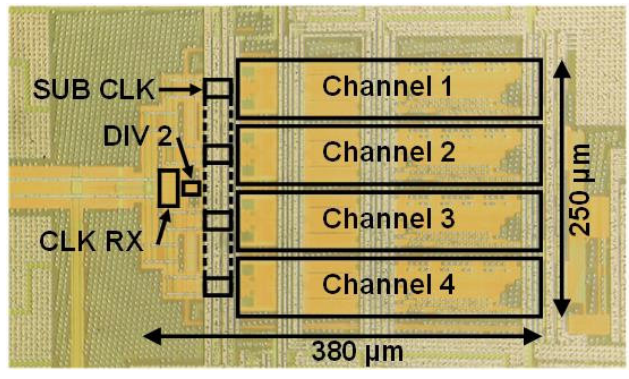


Fig. 2. Chip micrograph.

Publication(s)

[1] M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 4× interleaved 10GS/s 8b time-domain ADC with 16× interpolation-based inter-stage gain achieving >37.5dB SNDR at 18GHz input," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2020, pp. 252-253.

[2] M. Zhang, Y. Zhu, C. H. Chan, and R. P. Martins, "An 8-bit 10-GS/s 16× interpolation-based time-domain ADC with <1.5-ps uncalibrated quantization steps," IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3225-3235, Dec. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Single Channel GHz Sampling Rate Fully Dynamic Pipeline ADC

Zihao Zheng, Lai Wei, Jorge Lagos, Ewout Martens, Yan Zhu, Chi-Hang Chan, Jan Craninckx and Rui P. Martins

FEATURES

Sampling Rate > 3.3GHz
Single Channel Fastest Pipeline
Low power consumption, 5.5mW
On-chip calibrations
Fully dynamic power
Silicon verified in 28 nm CMOS

DESCRIPTION

This paper presents a single-channel 3.3 GS/s 6b pipelined ADC which features a post-amplification residue generation (PARG) scheme, linearized dynamic amplifier and on-chip calibration to achieve a high-speed, low-power, and compact prototype. The PARG scheme allows the quantization and amplification to run in parallel for a fast pipelining operation. The 6b ADC consists of 6 pipelined stages with 6 comparators and 5 amplifiers in total. Such small number of hardware reduces the overhead from the calibration and enables fully on-chip implementation. By further sharing the calibration hardware between the offset and gain calibration, the ADC with on-chip calibration only occupies 0.0166 mm² in 28 nm CMOS. With a linearized dynamic amplifier for the residue amplification, the ADC achieves 34 dB SNDR with a Nyquist input with 3.3 GS/s, consuming 5.5 mW and yielding a 40.02 fJ/conversion-step Walden FoM.

The ADC is fabricated in 28 nm CMOS, with ~40 fF input capacitance (excluding ESD) and occupies an active area of 0.0166 mm² (132 µm x 126 µm), including on-chip calibration. The input swing of the prototype is 400mVpp-diff to adopt the PARG scheme. During measurements, the on-chip calibration is performed at the foreground and the calibration counter values are frozen throughout all conditions. The measured output spectrum (decimated by 225) at 3.3 GS/s for an input near Nyquist (1.649 GHz), with and without calibration. Before the calibration, the 2nd and 3rd harmonic dominate the SFDR and greatly limit the achievable SNDR. The mismatches between differential circuits cause mainly the second harmonic, while the offset and gain error results in the third harmonic. These harmonics are reduced once the calibration is done, and the SFDR is improved by 5 dB. The measured DNL and INL before calibration are +1.48 / -1 LSB and +1.08 / -1.68 LSB, and after calibration are +1.08 / -0.85 LSB and +1.11 / -1.044 LSB respectively.

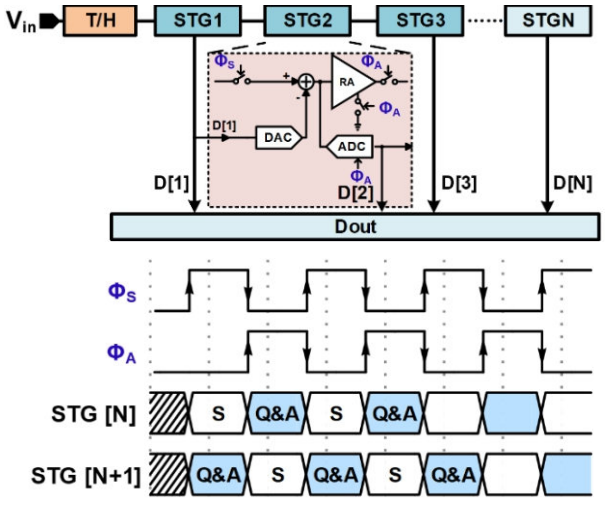


Fig. 1. Overall ADC Architecture and timing.

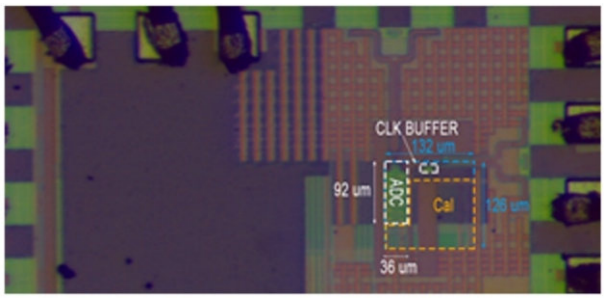


Fig. 2. Chip micrograph.

Publication(s)

[1] Z. Zheng et al., "16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 254-256.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 1.6GS/s 12.2mW 7/8-way Split Time-Interleaved SAR ADC achieving 54.2-dB SNDR with Digital Background Timing Mismatch Calibration

Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei, and Rui P. Martins

FEATURES

Novel Architecture: Split Time-Interleaved ADC

Relative prime Number Channels: 7/8 Way

Digital Background Timing Mismatch Calibration

High-speed: 1.6GS/s Sampling Rate

Wide-band:2.5-GHz effective resolution bandwidth

Low power consumption, 12.2 mW

Silicon verified in 28 nm CMOS

DESCRIPTION

It presents a split time-interleaved (TI) successive-approximation register (SAR) analog-to-digital converter (ADC) with digital background timing-skew mismatch calibration. It divides a TI-SAR ADC into two split parts with the same overall sampling rate but different numbers of TI channels. Benefitting from the proposed split TI topology, the timing skew calibration convergence speed is fast without any extra analog circuits. The input impedance of the overall TI-ADC remains unchanged, which is essential for the preceding driving stage in a high-speed application.

We designed a prototype 7/8-way split TI-ADC implemented in 28nm CMOS. After a digital background timing skew calibration, it reaches a 54.2 dB SNDR and 67.1 dB SFDR with a near Nyquist rate input signal and a 2.5GHz effective resolution bandwidth (ERBW). Furthermore, the power consumption of ADC core (mismatch calibration off-chip) is 12.2mW running at 1.6GS/s, leading to a Walden FOM of 18.2fJ/conv.-step and a Schreier FOM of 162.4dB, respectively.

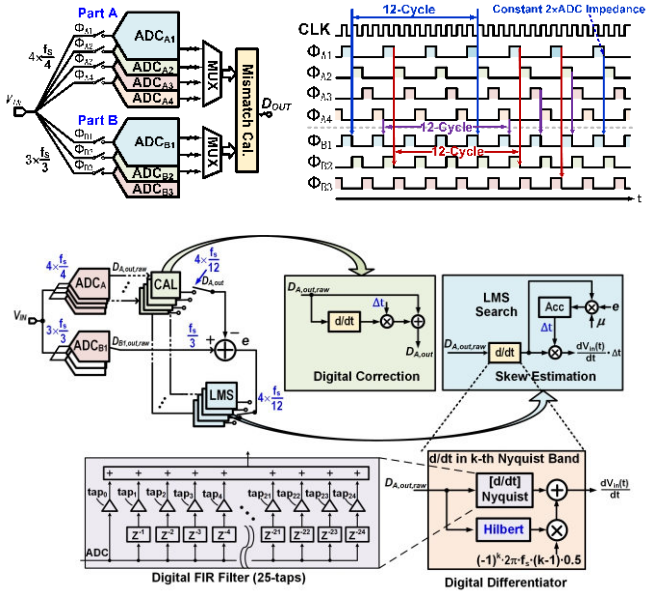


Fig. 1. The architecture and timing skew mismatch calibration of a 3/4-way split TI ADC

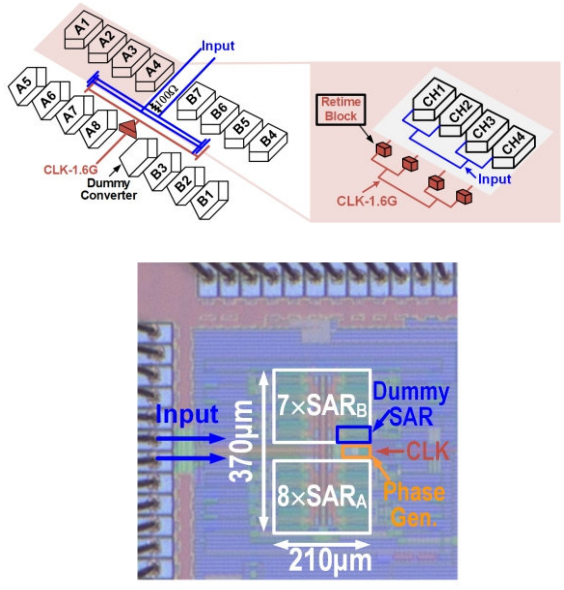


Fig. 2. Block diagram and chip micrograph of 7/8-way split TI ADC.

Publication(s)

[1] M. Guo, J. Mao, S. -W. Sin, H. Wei and R. P. Martins, "A 10b 1.6GS/s 12.2mW 7/8-way Split Time-interleaved SAR ADC with Digital Background Mismatch Calibration," 2019 IEEE Custom Integrated Circuits Conference (CICC), 2019, pp. 1-4.

[2] M. Guo, J. Mao, S. Sin, H. Wei and R. P. Martins, "A 1.6-GS/s 12.2-mW Seven-/Eight-Way Split Time-Interleaved SAR ADC Achieving 54.2-dB SNDR With Digital Background Timing Mismatch Calibration," IEEE Journal of Solid-State Circuits, vol. 55, no. 3, pp. 693-705, March 2020 (Invited Special Issue of CICC).

Sponsorship

Macau Science & Technology Fund (Ref: SKL-AMSV-2017-2019(DP)), Research Grants of University of Macau (Ref: MYRG2018-00204-AMSV).

A 5 GS/s 29 mW Interleaved SAR ADC Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications

Mingqiang Guo, Jiaji Mao, Sai-Weng Sin, Hegong Wei, and Rui P. Martins

FEATURES

Fully Digital Background Timing Mismatch Calibration

High-speed: 5GS/s Sampling Rate

Wide-band:4-GHz effective resolution bandwidth

Low power consumption, 29 mW

Silicon verified in 28 nm CMOS

DESCRIPTION

It presents a 16-channel 5 GS/s time-interleaved (TI) SAR ADC for a direct-sampling receiver that employs a digital-mixing background timing mismatch calibration to compensate for timing-skew errors. It uses a first-order approximation to obtain the derivative of the autocorrelation of the input signal, subsequently used to evaluate the explicit amount of the timing-skew. Therefore, this allows a digital background calibration of the timing-skew, avoiding extra analog circuits. The proposed 16-channel TI ADC uses a splitting-combined monotonic DAC switching method for the individual SAR channel to achieve a trade-off of simple switching and small common-mode voltage variation of the comparator.

The prototype is implemented in a 28 nm CMOS, reaches a 48.5/47.8 dB SNDR with an input signal of 2.38/4.0 GHz after the proposed background timing mismatch calibration, respectively. Furthermore, the ADC core's power consumption is 29 mW sampling at 5 GS/s, with a Walden FoM of 26.7 fJ/conv.-step and a Schreier FoM of 157.9 dB.

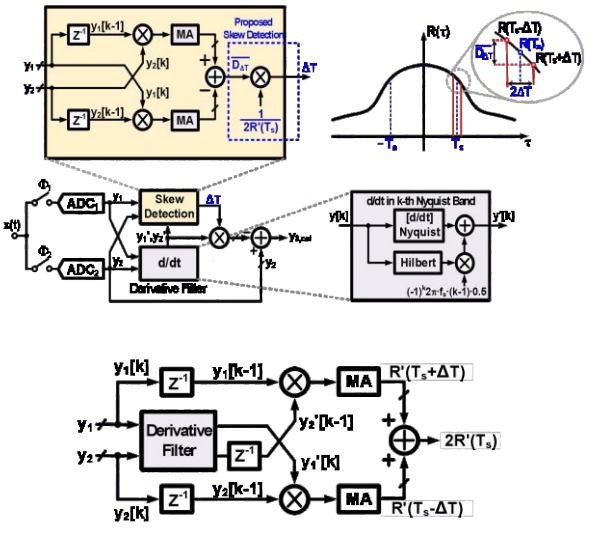


Fig. 1. Proposed fully digital timing mismatch topology based on digital-mixing.

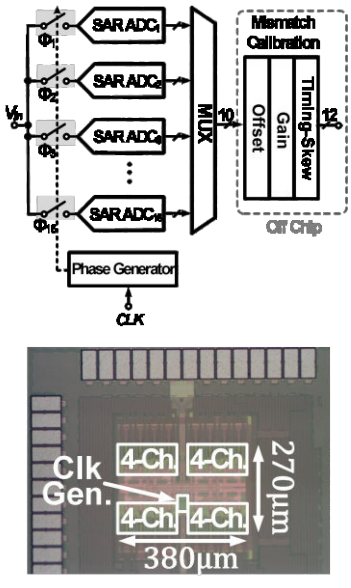


Fig. 2. Block diagram and chip micrograph f 16-way TI ADC.

Publication(s)

[1] M. Guo, J. Mao, S. -W. Sin, H. Wei and R. P. Martins, "A 29mW 5GS/s Time-interleaved SAR ADC achieving 48.5dB SNDR With Fully-Digital Timing-Skew Calibration Based on Digital-Mixing," 2019 Symposium on VLSI Circuits, 2019, pp. C76-C77.

[2] M. Guo, J. Mao, S. -W. Sin, H. Wei and R. P. Martins, "A 5 GS/s 29 mW Interleaved SAR ADC With 48.5 dB SNDR Using Digital-Mixing Background Timing-Skew Calibration for Direct Sampling Applications," IEEE Access, vol. 8, pp. 138944-138954, 2020.

Sponsorship

National Key R&D Program of China (File no. 2019YFB1310000), Macau Science and Technology Development Fund (FDCT, File no. SKL-AMSV(UM)-2020-2022), Research Committee of University of Macau (File no. MYRG2017-00192 -FST & MYRG2018-00204-AMSV).

A 3-stage GHz Sampling Rate Fully Dynamic Pipeline ADC

Wenning Jiang, Yan Zhu, Minglei Zhang, Chi-Hang Chan and Rui P. Martins

FEATURES

Sampling Rate > 1GHz
Single Channel Pipeline-SAR
Low power consumption, 7.6mW
VT Robust
Linearized fully-settled dynamic amplifier
Silicon verified in 28 nm CMOS

DESCRIPTION

A temperature-stabilized 12-bit single-channel SAR-assisted pipelined ADC running at 1 GS/s with Nyquist SNDR above 60 dB is presented. The ADC employs a 3-stage (4b-4b-6b) SAR-assisted pipeline hybrid architecture to achieve an attractive energy efficiency along with an extended sampling rate. A high-linearity open-loop Gm-R-based residue amplifier (RA) with both complete-settled and dynamic features improves the residue amplification efficiency and speed, while reducing the gain variation over a temperature drift. The inter-stage gain variation over the temperature is compensated through complementary temperature coefficients from the inner devices of the RA. Furthermore, a cascade amplification topology in the backend RA alleviates the effect of the input parasitic capacitance to its front-end capacitor DAC (CDAC), thus leading to a small CDAC size to accelerate amplification and conversion. The prototype ADC was fabricated in a 28-nm CMOS process and consumes 7.6 mW from a 1 V power supply at 1 GS/s.

The prototype ADC was fabricated in a 28-nm CMOS process, occupying a core area of 0.0091 mm². The ADC powered by a 1 V supply exhibits a 1.2 Vpp-diff full scale range. Due to the unskilled layout, the L-DAC suffers from some mismatch and a bit weight calibration is adopted in the measurement. The first 4b codes are corrected with integer bit weight one-time, and the bit weight array is fixed to different samples. Besides, the one-time calibration to the comparators offset (histogram-based detection in the measurement), RAs gain is done in the foreground. The measured DNL and INL are +0.47/-0.39 LSB and +1.87/-2.21 LSB, respectively. For a low input frequency of 140.63 MHz, the measured SNDR and SFDR are 61.4 dB and 74.6 dB, respectively, and the noise performance (SNR) is limited by the input buffer. For the near Nyquist input frequency of 495.19 MHz, the measured SNDR keeps 60 dB and the SFDR keeps 74.6 dB. The ADC achieves above 9b ENOB even with the input frequency raised up to 1.2 GHz, and the estimated clock jitter (~200 fs) degrades the dynamic performance when the input signal exceeds 1 GHz. The ADC keeps around 59 dB SNDR under 1.1 GS/s.

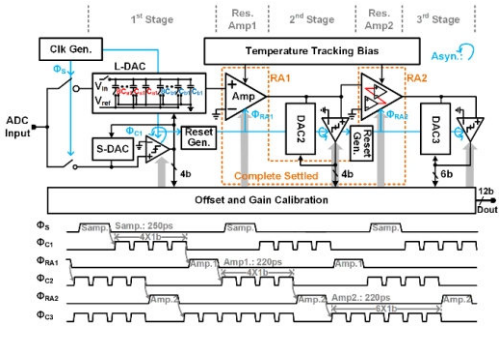


Fig. 1. Overall ADC Architecture and timing.

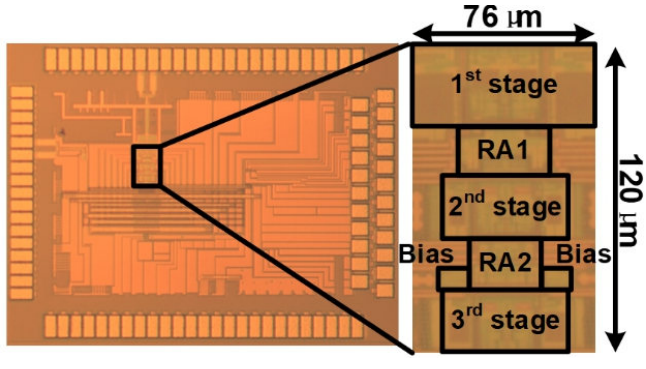


Fig. 2. Chip micrograph.

Publication(s)

[1] W. Jiang, Y. Zhu, M. Zhang, C. Chan and R. P. Martins, "3.2 A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 60-62, Feb. 2019.

[2] W. Jiang, Y. Zhu, M. Zhang, C. Chan and R. P. Martins, "A Temperature-Stabilized Single-Channel 1-GS/s 60-dB SNDR SAR-Assisted Pipelined ADC With Dynamic Gm-R-Based Amplifier," in IEEE Journal of Solid-State Circuits, vol. 55, no. 2, pp. 322-332, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

RESEARCH ABSTRACTS

Analog and Mixed-Signal Circuits

A 0.35-V 5,200-μm² 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator -------- 54

A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy-Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8μW Steady-State Power -------- 55

Startup time and energy-reduction techniques for crystal oscillators in the IoT era -------- 56

A Low Jitter Ring-based PLL over PVT -------- 57

A 0.35-V 5,200-µm² 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator

Ka-Meng Lei, Pui-In Mak, and Rui P. Martins

FEATURES

- Compact area of 5,200-µm²
- Ultra-low-voltage (0.35V) operation
- Novel asymmetric swing-boosted RC network
- Lowest energy efficiency (0.67 pJ/cycle) among the reported MHz-range relaxation oscillators

DESCRIPTION

For the crystal-less Internet-of-Things (IoT) node and wake-up receiver, low-power and fully integrated kHz-to-MHz clock sources with moderate frequency inaccuracy are pivotal to their operations. This projects develops a 2.1-MHz relaxation oscillator (RxO) for energy-harvesting Internet-of-Things (IoT) sensor nodes. The RxO features an asymmetric swing-boosted RC network and a dual-path comparator to surmount the challenges of sub-0.5-V operation while achieving temperature resilience. The former enables alternating the common-mode voltages at the output of the RC network to facilitate the sub-0.5-V operation, while the latter is outfitted with a delay generator for tracking the temperature-sensitive delay of the comparator.

Prototyped in 28-nm CMOS, the RxO occupies a tiny footprint of 5,200 µm². The power consumption is 1.4 µW at 0.35 V. The measured temperature stability is 158 ppm/°C (average of seven chips) over −20 ◦C–120 ◦C. It scores the best energy efficiency (667 fJ/cycle) among the reported MHz-range RxOs and has a figure-of-merit (181 dB) that compares favorably with the state-of-the-art, despite the ultra-low-voltage headroom and can settle within 3.6 µs after enabling the supply voltage.

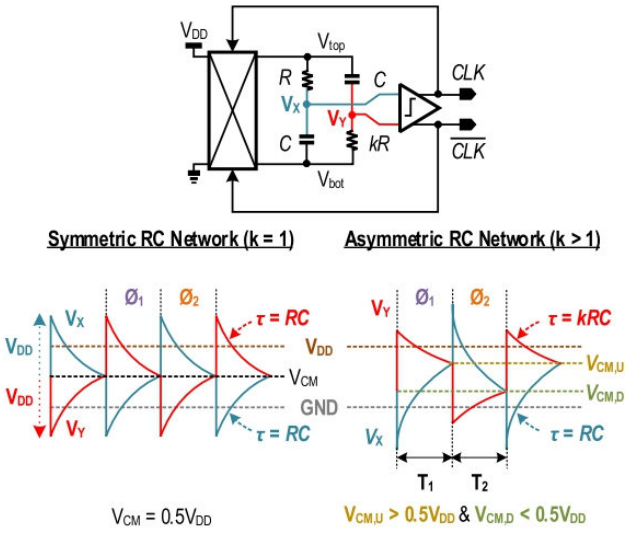


Fig. 1. Simplified schematic of the swing-boosted differential RxO and the design of k to maneuver VCM at different phases of operation.

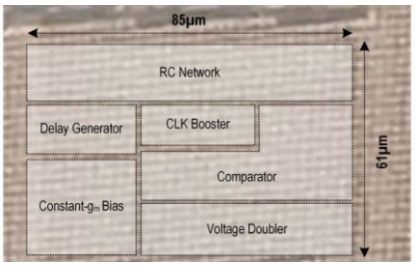


Fig. 2. Chip micrograph.

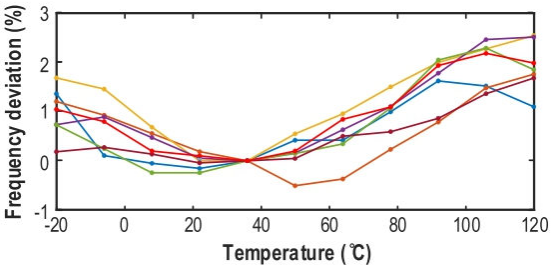


Fig. 3. Measured RxO's frequency stability versus temperature.

Publication(s)

[1] Ka-Meng Lei, Pui-In Mak, Rui P. Martins, "A 0.35-V 5,200-µm² 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator," IEEE Journal of Solid-State Circuits, Early Access, 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Regulation-Free Sub-0.5V 16/24MHz Crystal Oscillator for Energy-Harvesting BLE Radios with 14.2nJ Startup Energy and 31.8µW Steady-State Power

Ka-Meng Lei, Pui-In Mak, Man-Kay Law, and Rui P. Martins

FEATURES

Inductive multi-stage g_m for fast startup

Lowest operating voltage (0.35V) reported

Low startup energy of 14.2 nJ

Silicon verified in CMOS 65 nm process

DESCRIPTION

This project reports a regulation-free sub-0.5-V crystal oscillator (XO). The XO specifically designed for Bluetooth low-energy (BLE) radios aims for direct-powering by the harvested energy.

To secure its performance against process, voltage, and temperature (PVT) variations, while reducing its startup time and energy, we propose a dual-mode g_m scheme and a scalable self-reference chirp injection (SSCI) technique. The former employs an inductive multistage g_m to mitigate the crystal's stray capacitance during the startup, but a single-stage g_m in the steady state to preserve the phase noise (PN). For the latter (SSCI), we generate a scalable chirping sequence to kickstart the XO, avoiding trimming of the auxiliary oscillator.

The XO fabricated in 65-nm CMOS is measured with two common crystals (16/24 MHz) over a 0.3-to-0.5-V supply. At 24 MHz and 0.35 V, the startup time and energy of the XO are 400 µs and 14.2 nJ, respectively, while showing a steady-state power of 31.8 µW and a PN of −134 dBc/Hz at 1-kHz offset. The frequency stability is 14.1 ppm against temperature (−40 °C – 90 °C) and 17.9 ppm against voltage (0.3–0.5 V), both conform to the BLE standard (±50 ppm) with adequate margin.

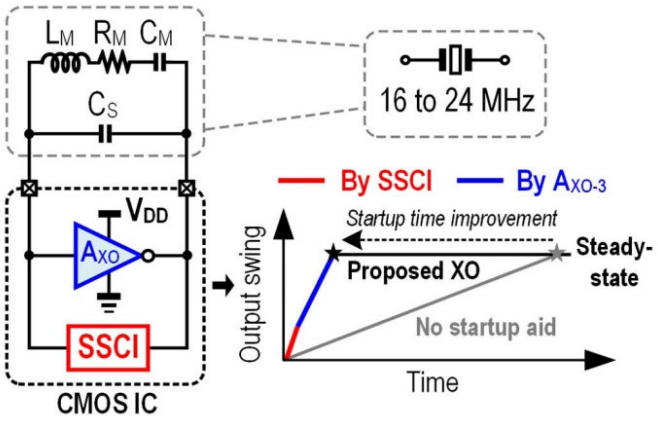


Fig. 1. Overview of the proposed XO and illustration of startup time improvement by two techniques: SSCI and inductive three-stage g_m.

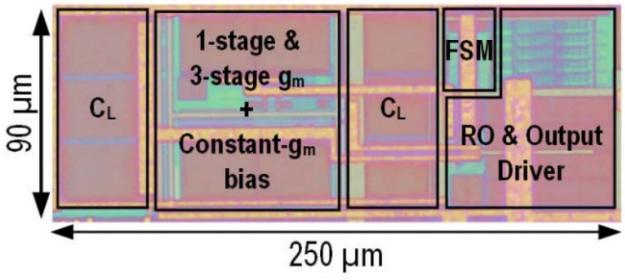


Fig. 2. Chip micrograph.

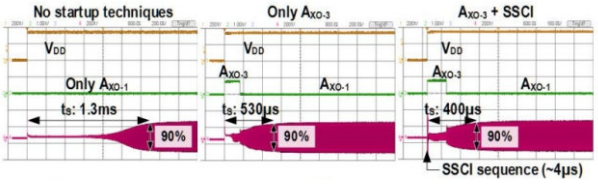


Fig. 3. Measured startup times with and without proposed techniques.

Publication(s)

[1] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8-µW steady-state power," IEEE J. Solid-State Circuits, vol. 53, no. 9, pp. 2624-2635, Sept. 2018.

[2] K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A regulation-free sub-0.5V 16/24MHz crystal oscillator for energy-harvesting BLE radios with 14.2nJ startup energy and 31.8µW steady-state power," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 52-53, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Startup time and energy-reduction techniques for crystal oscillators in the IoT era

Ka-Meng Lei, Pui-In Mak, and Rui P. Martins

FEATURES

Analyze startup time and energy reduction techniques for crystal oscillator

Classified into negative resistance boosting and energy injection

DESCRIPTION

Crystal oscillator (XO) is the *de facto* frequency reference of the modern wireless radios for its low power consumption, excellent phase noise (PN), and robustness against voltage and temperature variations. These essences come from the intrinsic high quality factor (Q ≈ 100,000) of the crystal. Yet, such a large Q also confines the startup time (t_s) of the XO. For example, a MHz-range XO takes a matter of milliseconds to reach the steady state. Long t_s was not a major concern for the conventional mobile devices, since the radio and XO are always on, or turned on for a long time compared with t_s. Facing the Internet-of-Things (IoT) era with massive wireless connectivity on objects, ultra-low-power (ULP) radios become crucial to extend the battery lifetime. Especially for the environmental monitoring, slow variation of ambient parameters (e.g., temperature and humidity) allows the use of duty-cycling to reduce the average power consumption. For instance, the Bluetooth Low Energy standard supports a 128-µs active mode every 1 s. During the sleep mode, the radio and XO are powered off, and long t_s can dominate the on-off latency of the radio. Also, the startup energy (E_S) of the XO limits the energy efficiency of the duty-cycled radio. As a result, recent efforts on XO for ULP IoT radios surge to improve both t_s and E_S.

In this Brief, we provide a mathematical treatment of the startup time of the crystal oscillator, and discuss the pros and cons of the recent startup time and energy-reduction techniques categorized as negative resistance boosting and energy injection.

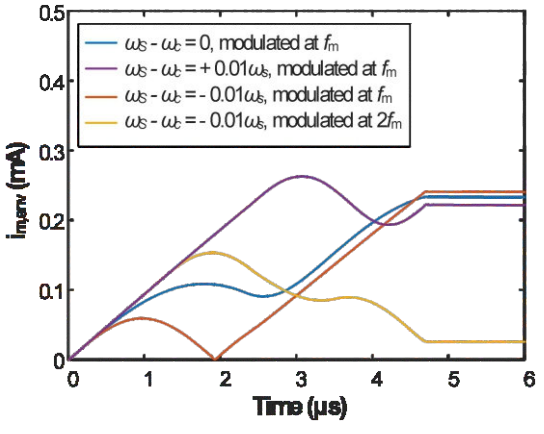


Fig. 1. The simulated $i_{M,env}$ of the 24MHz-crystal (L_M = 12 mH, C_M = 3.66 fF, R_M = 20 Ω) under different energy injection patterns and frequency mismatches (V_{INJ} = 1.2 V). The dithering signal modulated at f_m, which features a wider FWHM, guarantees a stable $i_{M,env}$ in the presence of frequency mismatch.

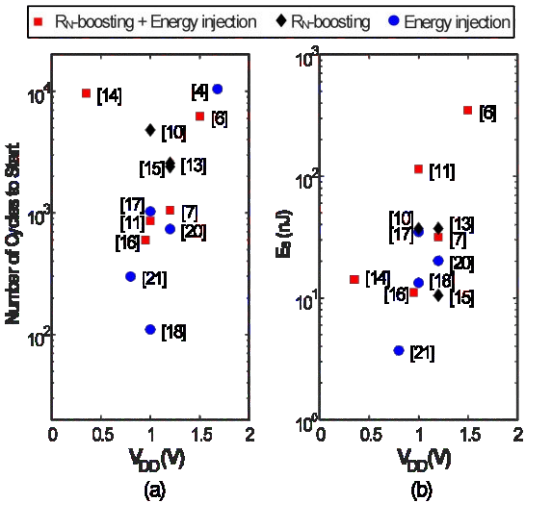


Fig. 2. Performance summary of recent XOs with t_s- and E_S-reduction techniques. (a) The number of cycles for the XO to start versus their V_{DD} (which limit the maximum V_{INJ}). (b) The E_S versus their V_{DD}.

Publication(s)

[1] Ka-Meng Lei, Pui-In Mak, Rui P. Martins, "Startup Time and Energy-Reduction Techniques for Crystal Oscillators in the IoT Era," IEEE Transactions on Circuits and Systems II, vol. 68, pp. 30-35, Jan. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

A Low Jitter Ring-based PLL over PVT

Xiaofeng Yang, Chi-Hang Chan, Yan Zhu and Rui P. Martins

FEATURES

Low jitter < 250fs
Ring-based PLL
Low power consumption, 4.1mW
PVT Robust
Phase Noise Cancellation
Silicon verified in 28 nm CMOS

DESCRIPTION

This paper presents a calibration-free and low-jitter phase-locked loop (PLL) with small performance degradation over PVT. We introduce an open-loop discrete-time phase noise cancellation (OPDTPNC) technique to achieve a wideband filtering and circuit inner-gain-tracking for PVT stabilization. The OPDTPNC is an effective phase realignment that enables a filtering bandwidth ~1/4 of the reference clock frequency. Besides, with the common structures and PVT tracking bias for sampler and corrector of the OPDTPNC, the prototype PLL maintains its low jitter under a wide range of PVT variations. Eventually, by cascading a Type-II PLL with the OPDTPNC, the proposed hybrid PLL attains the benefits of both Type-II PLL and injection-locked clock multiplier (ILCM). Fabricated in 28-nm CMOS with an active area of 0.023mm2 it consumes 4.1 mV from a 1 V supply with a reference spur of -63 dBc. The measured rms jitter of the 2.4 GHz PLL is 248 fs and 686 fs with and without OPDTPNC, respectively. When the temperature, supply and loop gain vary from 0 to 100℃, ±5%, and 6dB, respectively, the jitter performance only degrades less than 9%.

The proposed PLL with OPDTPNC, fabricated in 28nm CMOS, occupies an area of 0.023mm² The active area of the OPDTPNC block is 0.0016 mm2. The prototype PLL consumes a total of 4.1 mW, where the ring-VCO, PLL loop components and PNC consume 3.3 mW, 0.5 mW and 0.3 mW, respectively.

The measured phase noise of the reference clock and the 2.4 GHz output with and without the proposed PNC. We observe that the PNC circuit can suppress the phase noise significantly over a wide bandwidth. The integrated rms jitter of the PLL (10 KHz~100 MHz) is ~ 248 fs and 686 fs with and without the PNC, respectively; while the phase noise at 1 MHz frequency offset is -125.4 dBc/Hz and -109.3 dBc/Hz, respectively. The phase noise of the reference clock gets multiplied by 20·log(N), where N=16, and induces itself to the corrector's output directly without filtering. Therefore, the PN performance of the reference clock dominates the PLL clock at low and high frequency, which is similar to other PLLs based on the phase realignment scheme. There are closed-in spurs caused by the supply ripples as the RVCO is single-ended. Nevertheless, the proposed PNC also suppresses them due to the fast gain inner tracking mechanism. The measured reference spur with PNC is -63 dBc at 150 MHz offset frequency, while it is -62 dBc without PNC, both dominated by the supply cross-talk between the output buffer and reference clock buffer. We also measured the prototype PLL with different reference clock frequencies, and the integrated jitter is 234 fsrms with 156.25 MHz reference clock frequency.

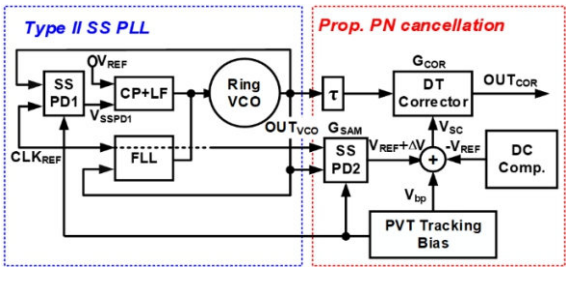


Fig. 1. Overall PLL Architecture.

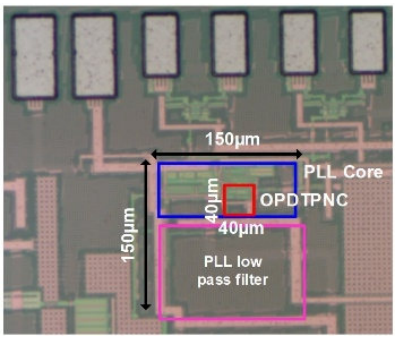


Fig. 2. Chip micrograph.

Publication(s)

[1] X. Yang, C. Chan, Y. Zhu and R. P. Martins, "A -246 dB Jitter-FoM 2.4 GHz Calibration-free Ring-Oscillator Achieving 9% Jitter Variation over PVT" in IEEE Int. Solid-State Circuits Conf. Dig. (ISSCC) Tech. Papers, pp. 260–261, Feb. 2019.

[2] X. Yang, C. -H. Chan, Y. Zhu and R. P. Martins, "A Calibration-Free Ring-Oscillator PLL With Gain Tracking Achieving 9% Jitter Variation Over PVT," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 3753-3763, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

RESEARCH ABSTRACTS

Biomedical Electronic Devices

Capacitive Micromachined Ultrasonic Transducer -------- 59

Fluorescence Immunochromatographic Assay Strip Readers -------- 60

Galvanic Coupling Intrabody Communication -------- 61

A Handheld High-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays -------- 62

Portable NMR with Parallelism -------- 63

An Integrated Circuit for Simultaneous Optogenetic Neural Manipulation and Electrophysiology Recording with Programmable 300mA LED/Laser Drivability -------- 64

Brain Rhythm Sequencing Using EEG Signals:A Case Study on Seizure Detection -------- 66

Low-latency single channel real-time neural spike sorting system based on template matching -------- 68

Capacitive Micromachined Ultrasonic Transducer

Sio Hang Pun and Mang I Vai

FOCUS ON

Analytical Modeling

High Frequency CMUT Design

POTENTIAL APPLICATIONS

Medical Imaging

Underwater Imaging

DESCRIPTION

Analytical modeling of CMUT is one of the commonly used modeling methods and has the advantages of intuitive understanding of the physics of CMUTs and convergent when modeling of collapse mode CMUT. Modeling of the membrane deflections are characterized by governing equations from Timoshenko, von Kármán equations and the 2D plate equation, and solved by various methods such as Galerkin's method and perturbation method. Analytical expressions from Timoshenko's equation can be used for small deflections, while analytical expression from von Kármán equations can be used for both small and large deflections. Building the model can be very helpful for understanding and designing CMUT with different requirements.

An embossed capacitive micromachined ultrasonic transducer (CMUT) is a device with embossed membrane that works in the collapse mode to improve output pressure in transmission. With the help from the modeling, a six-mask sacrificial release process is proposed for fabricating embossed CMUT arrays. Based on this process, the embossed pattern CMUTs were firstly fabricated. By using of electroplating methods, annular embossed patterns made of nickel were grown on the full top electrodes of CMUTs. The dimensions of the embossed pattern were about 3.0 μm in width and 1.4 μm in height. The resonant frequencies of the embossed CMUT array were 6.4MHz and 8.7MHz when the device worked in the conventional and the collapse mode, respectively.

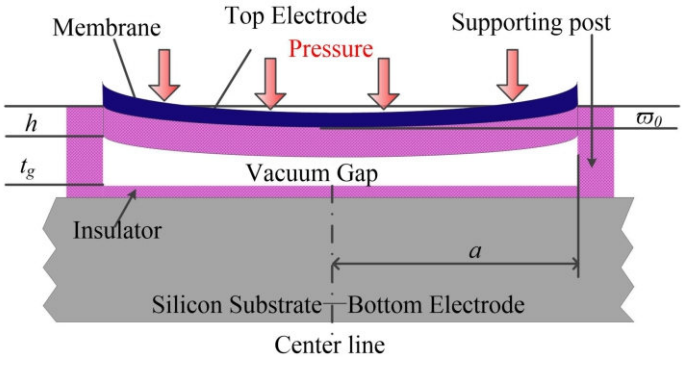


Fig. 1. The cross-sectional view of a collapse CMUT with full top electrode

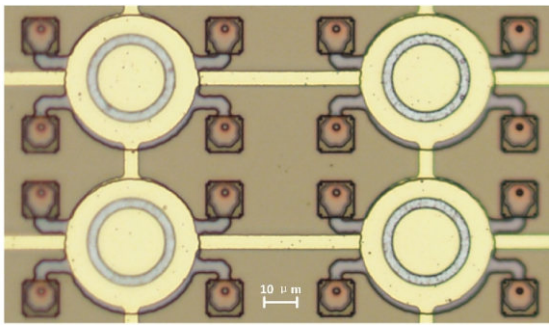


Fig. 2. Embossed CMUTs observed by an optical microscope

Publication(s)

[1] J Wang, X Liu, Y Yu, Y Li, C Cheng, S Zhang, P Mak, M Vai, S Pun, "A Review on Analytical Modeling for Collapse Mode Capacitive Micromachined Ultrasonic Transducer of the Collapse Voltage and the Static Membrane Deflections," Micromachines, vol. 12, no. 6, pp. 714, Jul 2021.

[2] Y Yu, J Wang, S Pun, C Cheng, K Lei, M Vai, S Zhang, P Mak, "Fabrication of embossed capacitive micromachined ultrasonic transducers using sacrificial release process," IEICE Electronics Express, vol 16, no 2, pp. 20181002-20181002, 2019

Sponsorship

National Natural Science Foundation of China, Chinese Ministry of Science and Technology, S&T Department of Fujian Province, FDCT, University of Macau

Fluorescence Immunochromatographic Assay Strip Readers

Sio Hang Pun and Mang I Vai

FEATURES

Detection range, 1-1024 µg/mL

Goodness of fit > 0.99

DESCRIPTION

Fluorescence immunochromatographic assay (FICA) is a quantitative detection technique widely used in clinical diagnosis, environmental monitoring, and food safety. To deal with the limited applications caused by insufficient detection range, a photoelectric adjustment system suitable for FICA strip readers to expand its detection was developed.

This photoelectric adjustment system is proposed based on the relationship between the excitation light intensity and the fluorescence intensity, which provides the optimal excitation light intensity and a stable baseline amplitude for the FICA strip reader.

The system was applied to the strip reader previously developed. The results show that the linear detection range of the FICA strip reader was extended from 1.95-256 µg/mL to 1-1024 µg/mL At the same time, the accuracy of the FICA strip reader does not deteriorate and is in good comparisons with the conventional ESEQuant Lateral Flow Reader (with R2 > 0.9987). The proposed photoelectric adjustment method and system can improve the detection range of the strip reader or other similar devices.

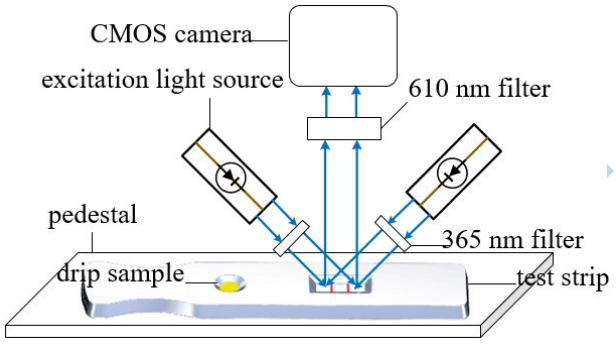


Fig. 1. Image acquisition device of the fluorescence immunochromatographic assay (FICA) reader based on image processing.

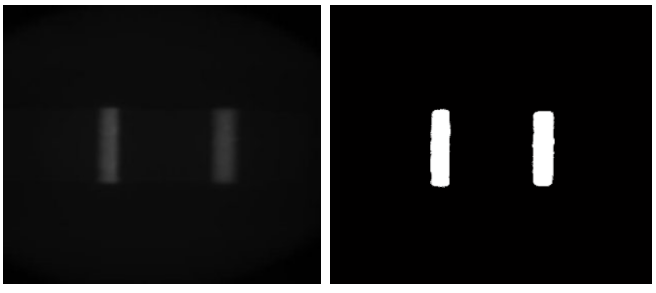


Fig. 2. 5. Results of image segmentation: left: original image; right: segmented image

Publication(s)

[1] H. Wu, Y. Gao, J. Yang, M. Vai, M. Du and S. Pun, "Development of a Photoelectric Adjustment System With Extended Range for Fluorescence Immunochromatographic Assay Strip Readers," in IEEE Photonics Journal, vol. 13, no. 3, pp. 1-12, June 2021, Art no. 6600512.

[2] Jiang R, Wu H, Yang J, Jiang H, Du M, Vai M, Pun S, Gao Y, “Automatic Range Adjustment of the Fluorescence Immunochromatographic Assay Based on Image Processing”, Sensors, 20(1):209, Dec. 2019.

Sponsorship

Chinese Ministry of Science and Technology, National Natural Science Foundation of China, Fujian Provincial Department of Science and Technology

Galvanic Coupling Intrabody Communication

Sio Hang Pun and Mang I Vai

POTENTIAL APPLICATIONS

In-Vivo Networking

Leadless Cardiac Pacemaker

DESCRIPTION

Galvanic coupling intrabody communication (IBC) is a low-power, low-cost wireless communication scheme that utilizes the human body as a medium to develop a body area network in IEEE 802.15.6.

Intrabody communication (IBC) can achieve better power efficiency and higher levels of security than other traditional wireless communication technologies. The existing IBC studies mainly focus on human channel characteristics of the physical layer, transceiver design for the application, and the protocol design for the networks. The human channel model used in most of the studies is just a multi-layer homocentric cylinder model.

Besides these, the majority of research on the body channel characteristics of galvanic coupling IBC are motionless and have only been evaluated in the frequency domain. Given the long measuring times of traditional methods, the access to dynamic variations and the simultaneous evaluation of the time-frequency domain remains a challenge for dynamic body channels such as the cardiac channel.

Our research tried to propose methods to accurately approximate the real human tissue layer and capturing dynamic variations in the body channel and provides a more comprehensive evaluation and richer information for the study of IBC.

To address this challenge, we proposed a parallel measurement methodology with a multi-tone strategy and a time-parameter processing approach to obtain a time-frequency evaluation for dynamic body channels. A group search algorithm has been performed to optimize the crest factor of multitone excitation in the time domain. To validate the proposed methods, in vivo experiments, with both dynamic and motionless conditions were measured using the traditional method and the proposed method. Most importantly, it is capable of capturing dynamic variations in the body channel and provides a more comprehensive evaluation and richer information for the study of IBC.

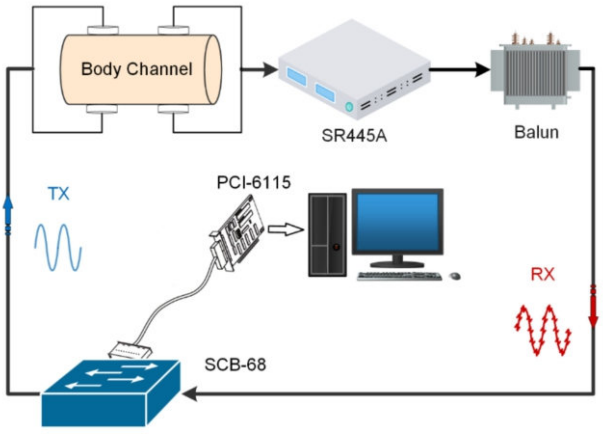


Fig. 1. Schematic diagram of experimental platform construction.

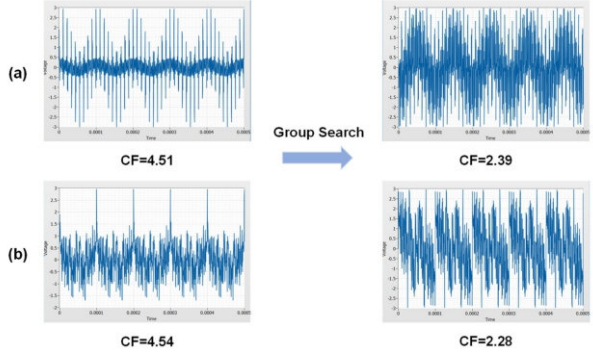


Fig. 2. The time domain waveform and its crest factors (CF) of the multitone before and after group search algorithm. (a) denotes linearly distributed multitone and (b) denotes quasi-logarithmically distributed multitone.

Publication(s)

[1] Z Wei, Y Wen, Y Gao, M Yang, J Yang, S Pun, M Vai, M Du, "A Time-Frequency Measurement and Evaluation Approach for Body Channel Characteristics in Galvanic Coupling Intrabody Communication," Sensors, vol. 21, no. 2, pp 348, Jan 2021

[2] Y Gao, Hi Zhang, S Lin, R Jiang, Z Chen, Ž Vasić, M Vai, M Du, M Cifrek, S Pun, "Electrical exposure analysis of galvanic-coupled intra-body communication based on the empirical arm models," Biomedical engineering online, vol. 17, no1, pp. 1-16, Dec 2018

Sponsorship

National Natural Science Foundation of China, Chinese Ministry of Science and Technology, S&T Department of Fujian Province, FDCT, University of Macau

A Handheld High-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays

Ka-Meng Lei, Hadi Heidari, Pui-In Mak, Man-Kay Law, F. Maloberti and R. P. Martins

FEATURES

First micro-NMR CMOS platform apt for multi-type biological/chemical assays

Low sample consumption (120× less)

Lightweight size (96× smaller and 175× smaller)

DESCRIPTION

We report a micro-nuclear magnetic resonance (NMR) system compatible with multi-type biological/chemical lab-on-a-chip assays. Unified in a handheld scale (dimension: 14 × 6 × 11 cm³, weight: 1.4 kg), the system is capable to detect <100 pM of Enterococcus faecalis derived DNA from a 2.5 µL sample.

The key components are a portable magnet (0.46 T, 1.25 kg) for nucleus magnetization, a system PCB for I/O interface, an FPGA for system control, a current driver for trimming the magnetic (B) field, and a silicon chip fabricated in 0.18 µm CMOS. The latter, integrated with a current-mode vertical Hall sensor and a low-noise readout circuit, facilitates closed-loop B-field stabilization (2 mT → 0.15 mT), which otherwise fluctuates with temperature or sample displacement. Together with a dynamic-B-field transceiver with a planar coil for micro-NMR assay and thermal control, the system demonstrates: 1) selective biological target pinpointing; 2) protein state analysis; and 3) solvent-polymer dynamics, suitable for healthcare, food and colloidal applications, respectively. Compared to a commercial NMR-assay product (Bruker mq-20), this platform greatly reduces the sample consumption (120×), hardware volume (175×), and weight (96×).

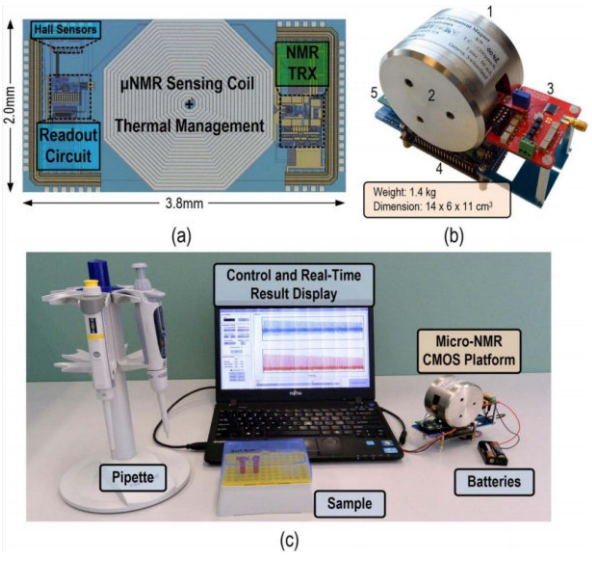


Fig. 1. (a) Chip photograph. (b) Prototype of the micro-NMR platform, including: 1) permanent magnet; 2) CMOS micro-NMR chip (inside magnet); 3) PCB; 4) FPGA and 5) current driver. (c) Experimental setup.

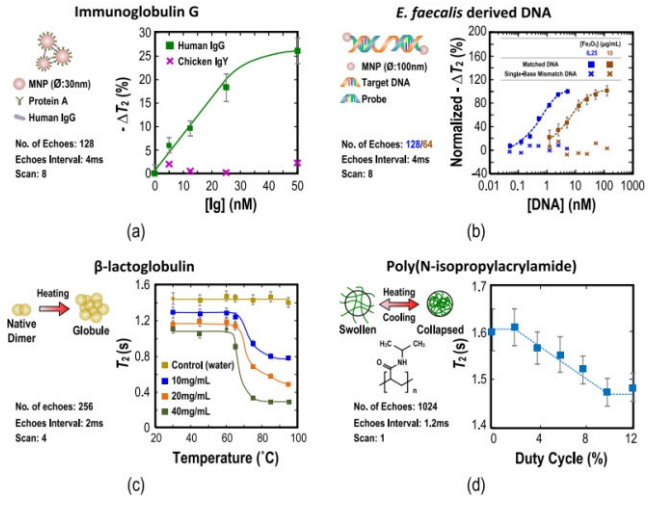


Fig. 2. Experimental results from biological/chemical samples. (a) Target quantification from human IgG as target and chicken IgY as control. (b) Target quantification from Enterococcus faecalis derived DNA together with single-base mismatch DNA. (c) Protein (β-LG) state detection with different heating temperature. (d) Polymer (PNIPAM) dynamics with the solvent during heating from the on-chip heater.

Publication(s)

[1] K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti, and R. P. Martins, "A Handheld High-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays," IEEE Journal of Solid-State Circuits, vol. 52, pp. 284-297, Jan. 2017.

[2] K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, R.P. Martins, and F. Maloberti, "A handheld 50pM-sensitivity micro-NMR CMOS platform with B-field stabilization for multi-type biological/chemical assays," in IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers, pp. 474-475, Feb. 2016

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Portable NMR with Parallelism

Ka Meng Lei, Dongwan Ha, Yi-Qiao Song, Robert Westervelt, Rui Martins, Pui-In Mak, and Donhee Ham

FEATURES

Portable NMR system featuring customized CMOS IC

Parallelized operation, reducing the overall experiments time

Shim coil to enhance the homogeneity and resolution

DESCRIPTION

Portable NMR combining a permanent magnet and a complementary metal-oxide-semiconductor (CMOS) integrated circuit has recently emerged to offer the long desired online, on-demand, or in situ NMR analysis of small molecules for chemistry and biology.

Here we take this cutting-edge technology to the next level by introducing parallelism to a state-of-the-art portable NMR platform to accelerate its experimental throughput, where NMR is notorious for inherently low throughput. With multiple (N) samples inside a single magnet, we perform simultaneous NMR analyses using a single silicon electronic chip, going beyond the traditional single-sample-per-magnet paradigm. We execute the parallel analyses via either time-interleaving or magnetic resonance imaging (MRI). In the time-interleaving method, the N samples occupy N separate NMR coils: we connect these N NMR coils to the single silicon chip one after another and repeat these sequential NMR scans. This time-interleaving is an effective parallelization, given a long recovery time of a single NMR scan.

To demonstrate this time-interleaved parallelism, we use N = 2 for high-resolution multidimensional spectroscopy such as J-coupling resolved free induction decay spectroscopy and correlation spectroscopy (COSY) with the field homogeneity carefully optimized (<0.16 ppm) and N = 4 for multidimensional relaxometry such as diffusion-edited T_2 mapping and T_1-T_2 correlation mapping, expediting the throughput by 2–4 times. In the MRI technique, the N samples (N = 18 in our demonstration) share 1 NMR coil connected to the single silicon chip and are imaged all at once multiple times, which reveals the relaxation time of all N samples simultaneously. This imaging-based approach accelerates the relaxation time measurement by 4.5 times, and it could be by 18 times if the signal-to-noise were not limited. Overall, this work demonstrates the first portable high-resolution multidimensional NMR with throughput-accelerating parallelism.

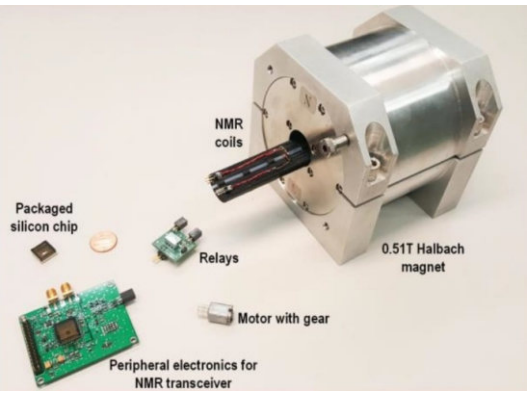


Fig. 1. Portable NMR with parallelism. Our portable NMR platform, whose key components are the Halbach magnet and the silicon IC we developed.

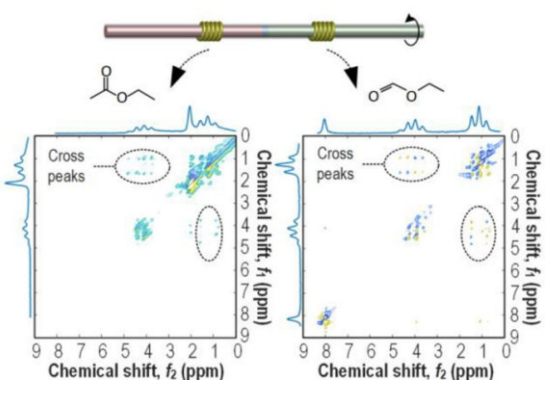


Fig. 2 Measured 2D ^{1}H NMR spectra with time-interleaving (2 NMR samples with 2 coils) from ethyl formate and ethyl acetate. Each sample undergoes 404 total scans.

Publication(s)

[1] Ka Meng Lei, Dongwan Ha, Yi-Qiao Song, Robert Westervelt, Rui Martins, Pui-In Mak, and Donhee Ham, “Portable NMR with Parallelism,” ACS Analytical Chemistry, 2020, 92, 2, 2112-2120.

Sponsorship

Macau Science and Technology Development Fund (FDCT).

An Integrated Circuit for Simultaneous Optogenetic Neural Manipulation and Electrophysiology Recording with Programmable 300mA LED/Laser Drivability

Chang Hao Chen, Elizabeth A McCullagh, Sio Hang Pun, Peng Un Mak, Mang I Vai, Mak Pui In , Achim Klug, Tim C. Lei

FEATURES

Optogenetic chip

low input capacitance of 9.7 pF

low input referred noise 4.57 μVrms

high driving current of 330 mA

DESCRIPTION

ELECTROPHYSIOLOGICAL recordings of action potentials in the brain have been one of the most important research tools available for neuroscientists to decipher the function of neuronal circuits. In addition to recording naturally occurring neuronal activity and to gain further insights into functions of these circuits, many neuroscientists desire to manipulate neuronal activity experimentally. One such method is the manipulation of neuronal circuits with light (optogenetics) to control complex neuronal functions, including behavior.

Several studies have been published regarding neural acquisition amplifier designs. However, most of these studies were focused on the ability to record from multiple electrodes, reduce power consumption, and improve the noise efficiency factor. The role of the amplifier's input impedance, which is one of the important parameters for extracellular recordings, has not received much attention in these designs. Tailoring the input impedances of amplifiers allows for selective measurements of local field potentials, action potentials from multiple neurons, or action potentials from a single neuron. In particular, a high impedance electrode with a small recording surface is necessary to record single neuronal activity and designs of neural amplifiers specially tailored for this application are relatively few.

We developed a monolithic IC that integrates a low-noise neural amplifier for action potential recording and a high current laser/LED driver for simultaneous optogenetic control to help meet the needs of this new and important trend of using optogenetics in neuroscience. In addition, an electrical noise model for the recording amplifier was derived to guide the amplifier design. In the model, noise sources from both the high impedance metal electrode and the optogenetic control process were included. The performance of the IC was tested with anesthetized Mongolian gerbils from which action potentials were recorded from the inferior colliculus in the midbrain. Additionally, we were able to inhibit spontaneous neural firings of the fifth nerve using optogenetics and an implantable "optrode" that includes a high input impedance electrode and the optical illumination fiber. Our results indicated that an integrated laser/LED controller can deliver a maximum current of 330 mA, which is adequate to effectively drive a laser to inhibit neural activity in the brainstem. The recording amplifier has a low input capacitance of 9.7 pF optimized for the use of high impedance electrodes for single cell extracellular recording. The input referred noise of the amplifier was measured to be 4.57 μVrms and the recorded action potentials had a signal-to-noise ratio of at least 6.6. Therefore, we believe that the use of this multi-functional IC system may reduce the complexities of using optogenetics with electrophysiology recording for current and future in-vivo and behavioral experiments to test various hypotheses in neuroscience.

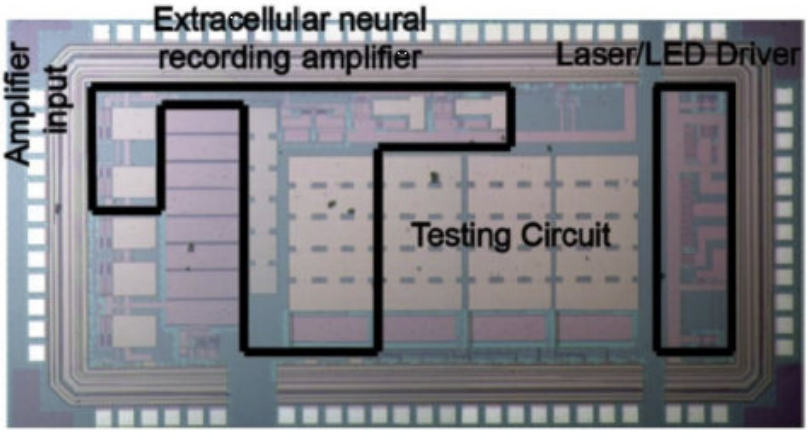


Figure A photograph of the fabricated IC with dimension of 2.9 mm × 1.6 mm. The actual neural amplifier and the laser/LED driver unit occupies about half of the space, with the rest of the space occupied by additional testing circuits.

Continuous

An Integrated Circuit for Simultaneous Optogenetic Neural Manipulation and Electrophysiology Recording with Programmable 300mA LED/Laser Drivability

Chang Hao Chen, Elizabeth A McCullagh, Sio Hang Pun, Peng Un Mak, Mang I Vai, Mak Pui In , Achim Klug, Tim C. Lei

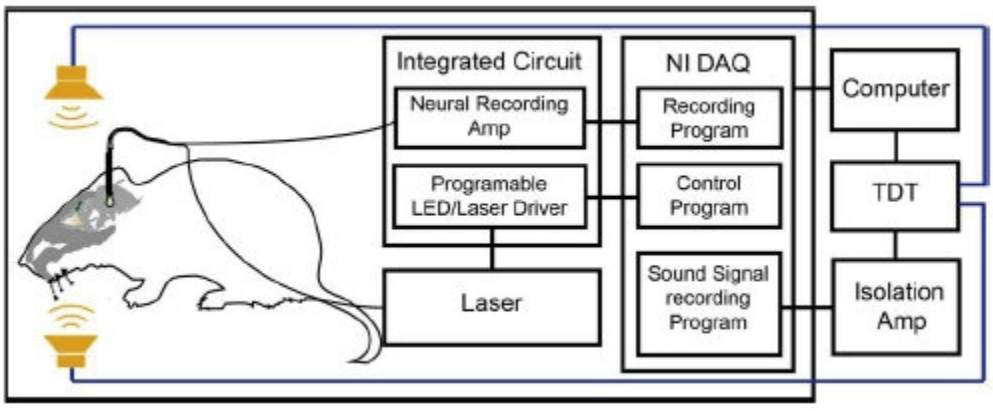


Figure 2 Experimental setup for simultaneous optogenetic inhibition and electrophysiological recordings from the brainstem of an anesthetized gerbil. The IC was connected to a data acquisition card (NI-DAQ) for signal digitization and laser power control. An isolation amplifier was used to isolate the neural amplifier from environmental noise. An audio signal processor (TDT) was used to generate a tonal signal to drive two speakers placed in the ears of the gerbil for auditory stimulation of the inferior colliculus.

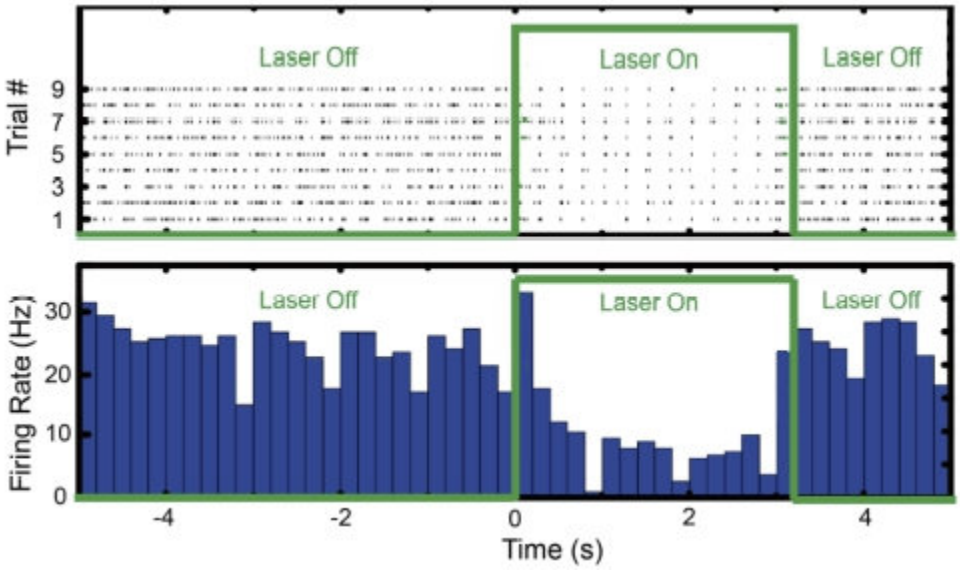


Figure 3 (A) Raster plot showing the temporal locations of action potential firing over nine optogenetic inhibition trials. (B) The calculated average firing rate showing significant reduction of the firing rate during optical illumination.

Publication(s)

Chen CH, McCullagh EA, Pun SH, et al. An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation. IEEE Trans Biomed Eng. 2017;64(3):557-568. doi:10.1109/TBME.2016.2609412

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Brain Rhythm Sequencing Using EEG Signals: A Case Study on Seizure Detection

Jia Wen Li, Shovan Barma, Peng Un Mak, Sio Hang Pun, and Mang I Vai

FEATURES

Low-latency real time neural spike sorting system

maximal spike sorting rate of 941 spikes/second

sorting latency less than 2 ms

DESCRIPTION

Brain rhythms are one series of trustworthy patterns that have been commonly employed for EEG-based applications. Moreover, they are generated from the classifications of EEG signals based on the five specific sub-bands: delta (δ, 0–4 Hz), theta(θ, 4–8 Hz), alpha (α, 8–13 Hz), beta (β, 13–30 Hz), and gamma (γ, 30–50 Hz). In fact, the effect of the brain rhythms is that the presence or change of certain brain rhythms can be considered as clues to recognize and detect mental diseases, neurological disorders, and affective reactions. For instance, the changes inαpower can significantly indicate sleep disorders. In Alzheimer's disease (AD), compared with the healthy subjects, the indications of amplitude increase in δ and θ sources, and the amplitude decrease in α and/or β sources can be detected in the patients. As for affective reactions, the changes of power in γ are usually related to happiness and sadness, α power varied with the level of valence, and so on. Categorically, the brain rhythms are deliberated as the fundamental or key components in the frequency domain representations of EEG signals. However, the rhythmic time behaviors, i.e., the indications and consecutive existences of the brain rhythms, which are useful information to interpret the EEG with great details, have not been investigated yet.

To study such chronological orders of the brain rhythms, the particular one which is appropriate to distinguish the specific brain state can be identified so that the details about the time-related transformations between different brain states can be determined. Meanwhile, the characteristics of the particular rhythm patterns are also useful for investigating the effect of subject-dependent in a specific brain state. On the other hand, based on the similarity measurement of the rhythm patterns among different channels, the signals synchrony in terms of rhythms synchronization can be indicated, which provides a solution to decrease the number of applied channels by mean of selecting several representatives. Thereby, to focus on the properties of the brain rhythms in their corresponding times of occurrences could extend the analysis and characterization of EEG signals in a new way. Then, inspired by the sequence analysis in bioinformatics, a technique named brain rhythm sequencing which interprets and characterizes the EEG as the sequence data consisted of the five specific brain rhythms has been proposed in this work. Moreover, this idea can be tested and employed for various EEG-based applications such as the detections of some neurological disorders.

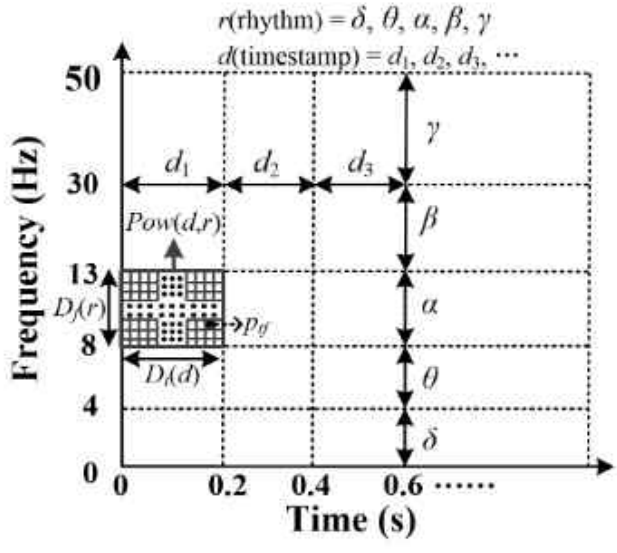


Figure 1 Power estimation of five brain rhythms at each timestamp by TFA (RSPWVD method); where r and d correspond to brain rhythm and time stamp respectively ; Pow(d,r) presents the power value of one specific rhythm at a certain timestamp; ptf indicates the instantaneous power in each bound of the time-frequency plane; Dt(d) and Df® is the distance between adjacent timestamps and brain rhythms separately

Continuous

Brain Rhythm Sequencing Using EEG Signals: A Case Study on Seizure Detection

Jia Wen Li, Shovan Barma, Peng Un Mak, Sio Hang Pun, and Mang I Vai

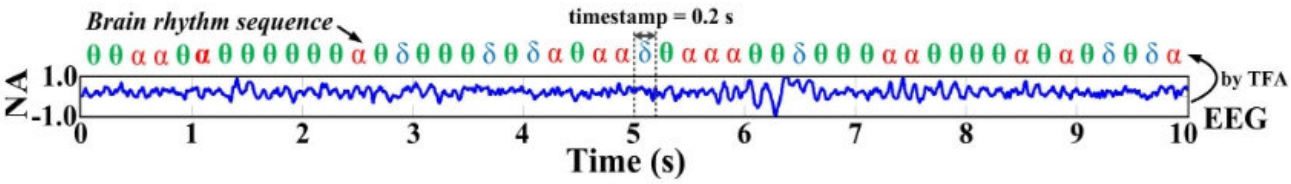


Figure 2 Brain rhythm sequencing from EEG signals based on choosing the prominent rhythm having the maximum power contribution at each timestamp of 0.2 s by TFA. Label: NA refers to normalized amplitude.

Channel	Coherence	Correlation	Mutual information	Rhythm sequencing
FP2	23.66%	21.51%	31.18%	24.73%
F4	**84.95%**	**81.72%**	**82.80%**	**74.19%**
C4	**83.87%**	**80.65%**	**79.57%**	**73.12%**
P4	**60.22%**	**68.82%**	**63.44%**	**64.52%**
F8	6.45%	13.98%	10.75%	12.90%
T4	**66.67%**	**59.14%**	**52.69%**	**60.22%**
T6	7.53%	11.83%	5.38%	8.60%
O2	4.30%	11.83%	6.45%	4.30%
FP1	2.15%	5.38%	9.68%	10.75%
F3	5.38%	1.08%	3.23%	7.53%
C3	8.60%	9.68%	3.23%	11.83%
P3	6.45%	2.15%	7.53%	9.68%
F7	0.00%	1.08%	1.08%	0.00%
T3	3.23%	6.45%	4.30%	7.53%
T5	0.00%	1.08%	4.30%	1.08%
O1	2.15%	0.00%	3.23%	1.08%

Figure 3 Results of representative channels based on proportions.

Publication(s)

J. W. Li, S. Barma, P. U. Mak, S. H. Pun and M. I. Vai, "Brain Rhythm Sequencing Using EEG Signals: A Case Study on Seizure Detection," in IEEE Access, vol. 7, pp. 160112-160124, 2019, doi: 10.1109/ACCESS.2019.2951376.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Low-latency single channel real-time neural spike sorting system based on template matching

Pan Ke Wang, Sio Hang Pun, Chang Hao Chen, Elizabeth A. McCullagh, Achim Klug, Anan Li, Mang I. Vai, Peng Un Mak, Tim C. Lei

FEATURES

Low-latency real time neural spike sorting system

maximal spike sorting rate of 941 spikes/second

sorting latency less than 2 ms

DESCRIPTION

Recording action potentials from neurons in the brain gives neuroscientists the ability to study neural circuits with single cell accuracy. Typically neural spikes (or action potentials) are recorded extracellularly with a metal or glass electrode inserted into the brain of an animal or a human patient. By contrast, intracellular or patch clamp recordings with glass pipettes are much less common in vivo because pulsation, movement of brain tissue and electrode contamination make them very challenging. Therefore, electrodes are typically placed within the extracellular space between neurons to capture neural spikes extracellularly. In this extracellular configuration, neural spikes generated from several adjacent neurons are often captured by the electrode at the same time, hereafter referred to as multi-units, making it challenging to determine the activity patterns of single neurons included in the recording. These multi-unit recordings are especially common when signals are measured from brain areas densely packed with neurons. For this reason, spike sorting algorithms are often used off-line to separate the neural spikes and assign them to different cluster groups. The underlying principle of spike sorting relies on the fact that neural spikes originating from different neurons will have different temporal profiles. The temporal profiles of these neural spikes are dependent on the impedance of the extracellular fluid between the neurons and the electrode, the currents produced by each neuron, as well as the cell membrane area from which the ionic currents can reach the metal electrode.

There has been a sustained effort to develop better spike sorting algorithms aimed at increasing both the accuracy and the speed of the sorting process. From a mathematical perspective, spike sorting can be considered as an unsupervised classification problem, and several classification algorithms, including K-means, Expectation Maximization (EM) and Multivariate Gaussian Mixture, have been used to sort neural spikes. Besides these classification algorithms, superparamagnetic clustering (SPC) was specifically designed for neural spike sorting [9]. SPC borrows the physical concept of magnetic thermal interaction and models neural spikes as magnetic spin elements. As the temperature rises, the neural spin elements fracture into distinct groups for spike classification. Aksenova et al. modeled neural spikes as self-oscillating nonlinear oscillators and can be expressed by trajectories in the phase space described by a perturbated ordinary differential equation. Caro-Martin et al also extracted linear independent spike features based on shape, phase and distribution features for the spikes and sort neural spikes using the spike features based on a modified k-mean technique. The advantage of using phase space features instead of temporal shapes to sort neural spikes is less prone to amplitude fluctuation and non-Gaussian distributed cluster structures. In addition, there are several other off-line spike sorting algorithms that the clustering is based on consensus-based modified k-mean techniques, variational Bayes, and maximum a posteriori to improve sorting speed and accuracy.

This work builds upon our previous results to develop a low sorting latency and high throughput spike sorting unit on a field programmable gate array (FPGA), assisted by a desktop computer. Our FPGA has the capability to perform real-time spike sorting by matching cluster templates pre-calculated by the desktop computer with neural spikes collected during a short training period. In order to ensure proper template generation, the templates were generated by a desktop computer using a more sophisticated neural spike sorting algorithm—SPC. The cluster templates were then transferred to the FPGA module for subsequent real-time spike sorting through matching the incoming neural spikes to these cluster templates. In order to allow the FPGA to achieve optimal sorting accuracy under different noisy conditions, two template matching methods–Euclidean distance (ED) and correlational matching (CM)–were also implemented in the FPGA and the two methods are selectable by investigators to achieve optimal sorting accuracy according to the type of noise during experiments. Rigorous testing determined that ED yield slightly better sorting accuracy when the spikes are contaminated by Gaussian noise. CM, on the other hand, can handle spike amplitude fluctuations caused by the metal electrode slowly drifting away from its initial implanted

Continuous

Low-latency single channel real-time neural spike sorting system based on template matching

Pan Ke Wang, Sio Hang Pun, Chang Hao Chen, Elizabeth A. McCullagh, Achim Klug, Anan Li, Mang I. Vai, Peng Un Mak, Tim C. Lei

position within the brain better, such as in long-term (minutes to hours) behavioral neuroscience studies performed on awake behaving animals. The algorithm was also compared with several off-line spike sorting algorithms indicating that the template matching technique achieves comparable sorting accuracies but has a three order-of-magnitude shorter sorting time.

With our approach, a maximal spike sorting rate of 941 spikes/second was achieved for a single electrode. This sorting rate is several times higher than the typical firing rates of neurons, preventing accidental loss of neural spikes in the sorting. The sorting latency of processing a neural spike was measured to be less than 2 ms, which should be fast enough to be used to analyze neural spike data in closed-loop neural control settings. The sorting rate and latency are approaching the theoretical limits set since the natural spike width of an action potential is ~1 ms, making the theoretical maximum sorting rate ~1000 spikes/second for a single electrode. In addition, the FPGA can also handle a maximum of eight neural clusters, which is generally more than the number of neurons a middle to high impedance metal electrode can simultaneously record.

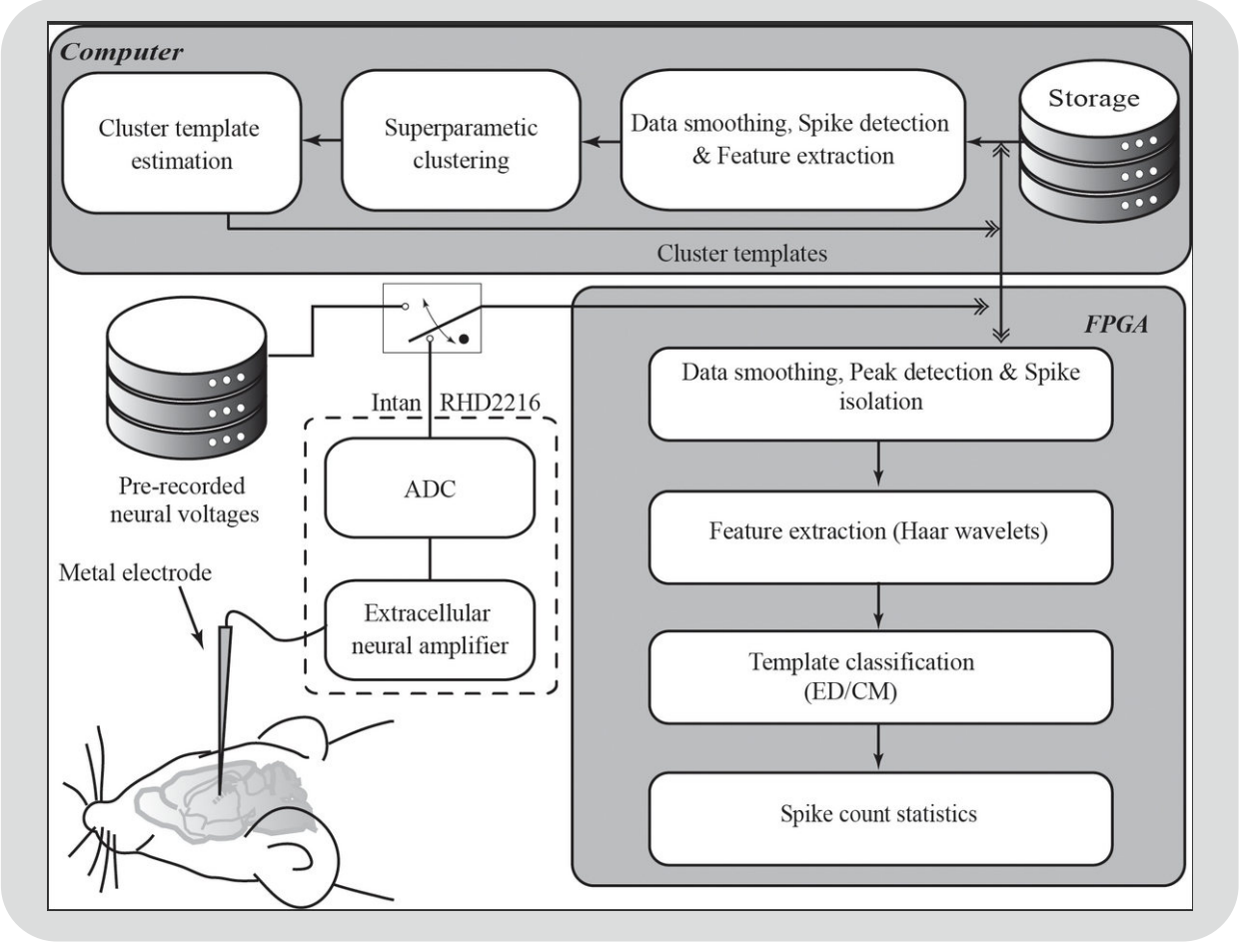


Figure 1 Block diagram of the real-time spike sorting system.

The system is comprised of a desktop computer and an FPGA module. The system can measure extracellular neural spikes from an animal with a neural amplifier and an analog-to-digital converter (ADC), or alternatively be directly injected with digitized pre-recorded neural voltages for system testing. The desktop computer contains three sub-processing units– 1) raw data smoothing, spike detection and feature extraction, 2) spike sorting using SPC and 3) template estimation. The FPGA module also contains four sub-processing units– 1) raw data smoothing, peak detection and spike isolation, 2) feature extraction, 3) neural spike sorting based on template matching, and 4) calculation of spike count statistics.

Continuous

Low-latency single channel real-time neural spike sorting system based on template matching

Pan Ke Wang, Sio Hang Pun, Chang Hao Chen, Elizabeth A. McCullagh, Achim Klug, Anan Li, Mang I. Vai, Peng Un Mak, Tim C. Lei

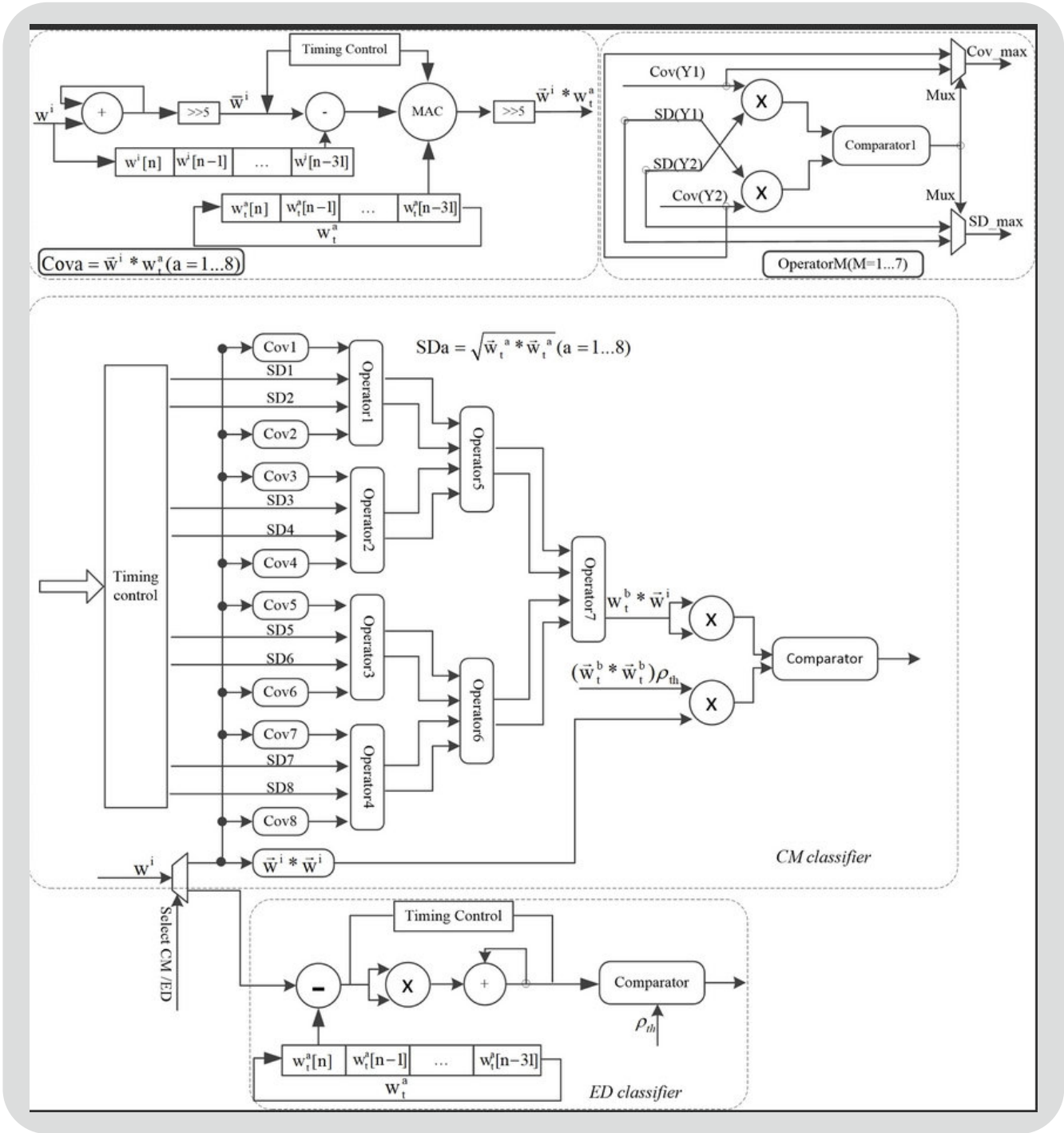


Figure 2 Hardware implementation of the CM and ED classifiers. Investigators can select one of the two classifiers through the “Select CM/ED” pin. Within the CM classifier, there are in total 8 covariance units (Cova) and 7 operator units (OperatorM) for determining the maximum correlation coefficient for the incoming spike to the eight cluster templates. Based on this design, the covariance calculations are performed in parallel to achieve minimum calculation latency. The hardware implementation of the covariance units, the operator units, and the ED classifier are also shown in detail on the top two sections and the bottom section of the figure.

Continuous

Low-latency single channel real-time neural spike sorting system based on template matching

Pan Ke Wang, Sio Hang Pun, Chang Hao Chen, Elizabeth A. McCullagh, Achim Klug, Anan Li, Mang I. Vai, Peng Un Mak, Tim C. Lei

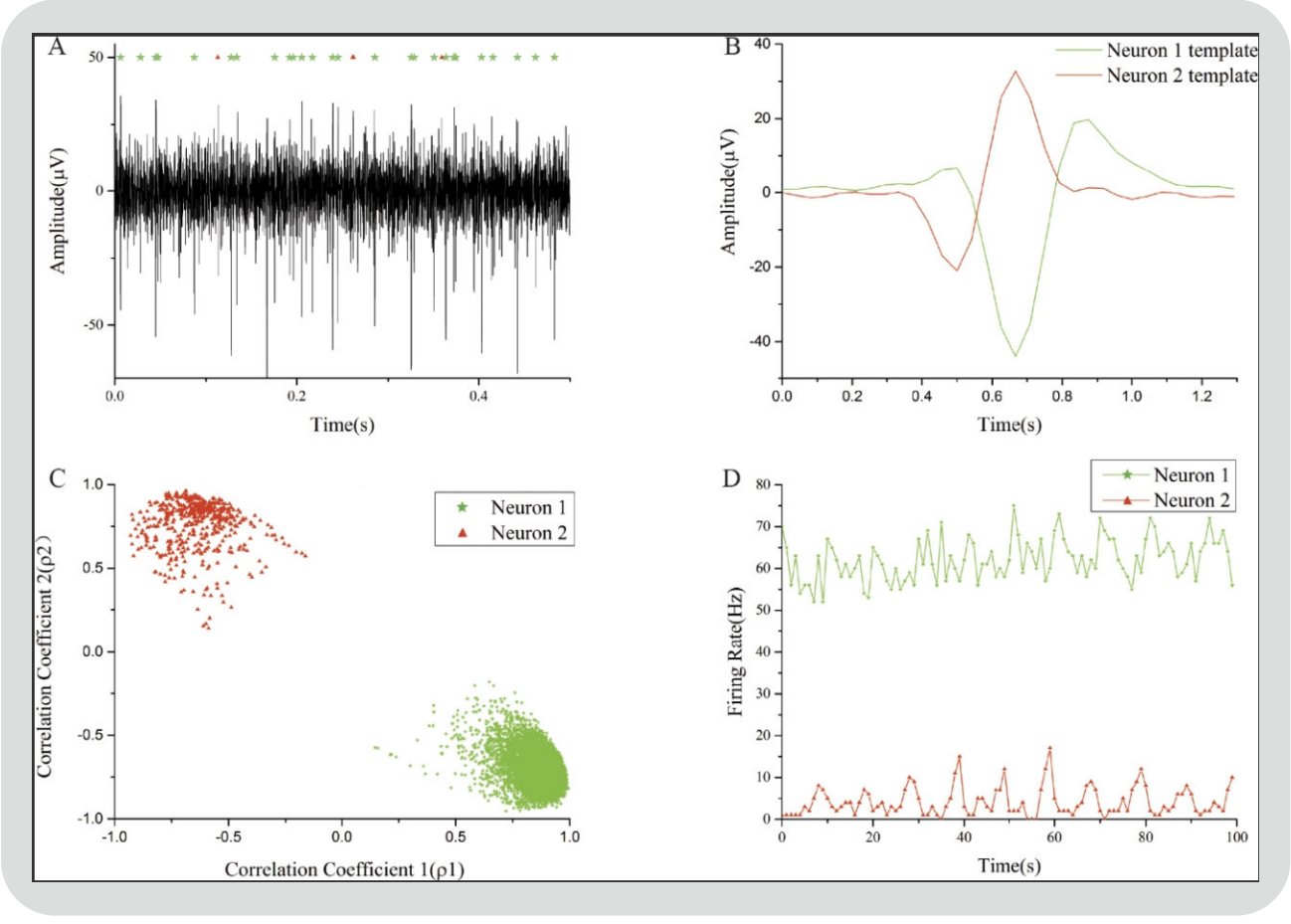


Figure 3 Real-time spike sorting results based on pre-recorded neural spikes from an anesthetized gerbil. (A) 0.5 s of neural voltage trace recorded from the brain stem of an anesthetized gerbil. The green stars and red triangles at the top of the figure indicate the locations of neural spikes of two neurons co-recorded by the same electrode. (B) Temporal profiles of the two cluster templates of the two neurons estimated by SPC. (C) Phase plot of the two cluster groups (green star and red triangle) with each marker representing a neural spike. (D) The firing rates of the two clusters calculated over the 100 seconds of neural data by the FPGA hardware

Publication(s)

Wang PK, Pun SH, Chen CH, McCullagh EA, Klug A, Li A, et al. (2019) Low-latency single channel real-time neural spike sorting system based on template matching. PLoS ONE 14(11): e0225138. https://doi.org/10.1371/journal.pone.0225138

Wang, Pan Ke; Chen, Chang Hao; Pun, Sio Hang; Zhang, Baijun; Mak, Peng Un; Vai, Mang I.; Lei, Tim C.: ' Parallelarchitecture to accelerate superparamagnetic clustering algorithm', Electronics Letters, 2020, 56, (14), p. 701-704, DOI:10.1049/el.2020.0760

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, National Natural Science Foundation of China, National Institutes of Health (NIH) Grant USA

RESEARCH ABSTRACTS

Energy Harvesting and Sensing Circuits

A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm² -------- 73

A 1.7mm² Inductor-less Fully-Integrated Capacitive-Flip Rectifier (CFR) for Piezoelectric Energy Harvesting with 483% Power Extraction Improvement -------- 74

A 4µm Diameter SPAD Using Less-doped N-Well Guard Ring in Baseline 65nm CMOS -------- 75

A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement -------- 76

A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes for Biomedical Implant Applications -------- 77

Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter with Wide Input Voltage Range and Enhanced Power Density -------- 78

A 0.22-to-2.4V-Input Fine-Grained Fully Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Achieving 84.1% Peak Efficiency at 13.2mW/mm²

Yang Jiang, Man-Kay Law, Pui-In Mak, Rui P. Martins

FEATURES

- Systematic algorithmic voltage feed-in topology for flexible rational VCR generation
- Efficient fully integrated SC DC-DC boost conversion
- Optimal conduction and reduced parasitic loss
- Total 24 VCRs at 84.1% η_{peak} and 13.4mW/mm²
- Silicon verified in standard 180 nm CMOS

DESCRIPTION

The work proposed an algorithmic voltage-feed-in (AVFI) topology capable of systematic generation of any arbitrary buck-boost rational ratio with optimal conduction loss while achieving reduced topology level parasitic loss among the state-of-the-art works. By disengaging the existing topology-level restrictions, we develop a cell-level implementation using the extracted Dickson cell (DSC) and charge-path-folding cell (QFC) to minimize the power stage parasitic loss, exhibiting a Dickson-like switching pattern. The proposed partitionable main cell (MC) and auxiliary cell (AC) architecture achieves fined-grained voltage conversion ratio (FVCR) reconfiguration with optimal power cell utilization and reduced control complexity.

Implemented in 65nm bulk CMOS, the fully integrated switched-capacitor power converter (SCPC) using 10 MCs and 10 ACs executes a total of 24 VCRs (11 buck and 13 boost) with wide-range efficient buck-boost operations through the proposed reference-selective bootstrapping driver (RSBD). Based on the AVFI topology, the chip prototype reaches a measured peak efficiency of 84.1% at a power density of 13.4 mW/mm² over a wide range of input (0.22-to-2.4V) and output (0.85-to-1.2V).

Benchmarking with the prior art, this work achieves a significant power density improvement except from those using special processes. It also demonstrates an increased number of VCRs and a higher peak efficiency, as well as an improved power density by >13× when compared with the state-of-the-art buck-boost SCPCs.

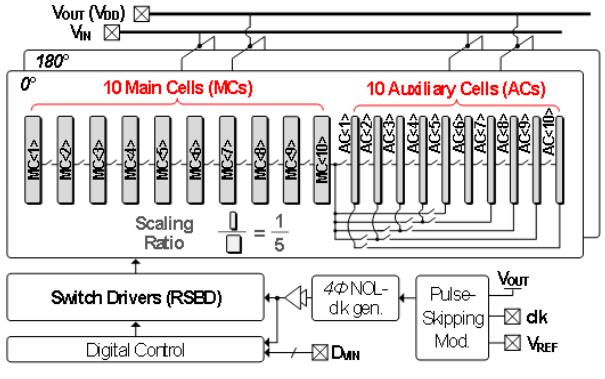


Fig. 1. System overview of the implemented ASP SC boost converter.

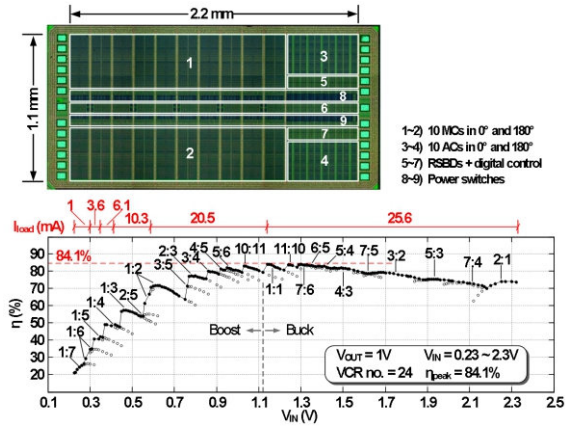


Fig. 2. Chip micrograph and measured efficiency at VOUT=1V over a wide V_{IN} range.

Publication(s)

[1] Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters," IEEE Journal of Solid-State Circuits, vol. 53, no. 12, pp. 3455-3469, Dec. 2018.

[2] Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "A 0.22-to-2.4V-Input Fine-Grained Fully-Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Archiving 84.1% Peak Efficiency at 13.2mW/mm²," IEEE International Solid-State Circuit Conference (ISSCC), Digest of Technical Papers, pp. 422-423, Feb. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 1.7mm² Inductor-less Fully-Integrated Capacitive-Flip Rectifier (CFR) for Piezoelectric Energy Harvesting with 483% Power Extraction Improvement

Zhiyuan Chen, Yang Jiang, Man-Kay Law, Pui-In Mak, Xiaoyang Zeng, Rui P. Martins

FEATURES

Efficient energy extraction using FCR

Fully-Integrated PEH Interface with no off-chip Inductor

7-phase operation with reconfiguration capacitor array

Wide input power adaptation

Loss optimization among phase offset, incomplete charge transfer and reduced conduction time

Silicon verified in standard 180 nm 1.8/3.3/6V CMOS

DESCRIPTION

The work presents a fully-integrated piezoelectric energy harvesting interface without external components. Instead of relying on bulky external inductors with high quality factor as in the conventional parallel-synchronized-switch harvesting-on-inductor (P-SSHI) approach, we propose a flipping-capacitor rectifier (FCR) topology to achieve voltage inversion of the piezoelectric energy harvester (PEH) through a reconfigurable capacitor array. This fundamentally preserves a fully-integrated solution without inductors while achieving a high energy extraction capability. Measurement results from FCR1 using discrete components shows an output power enhancement of up to 3.4x, which is close to the theoretical prediction.

We fabricated also a 7-phase FCR3 with 4 MIM capacitors and 21 switches using a 0.18-µm 1.8/3.3/6V CMOS process, occupying an active area of ~1.7 mm². Additionally, we implemented an active rectifier based on a common-gate comparator with phase alignment to ensure high speed operation while minimizing the diode voltage drop. A phase generate-and-combine circuit eliminates redundant switching activities.

Benchmarking with the prior art, this work reports the first PEH interface that exhibits a high MOPIR (4.83x) and high voltage flipping efficnecy (η_F) of 0.85 in a compact area with zero external components.

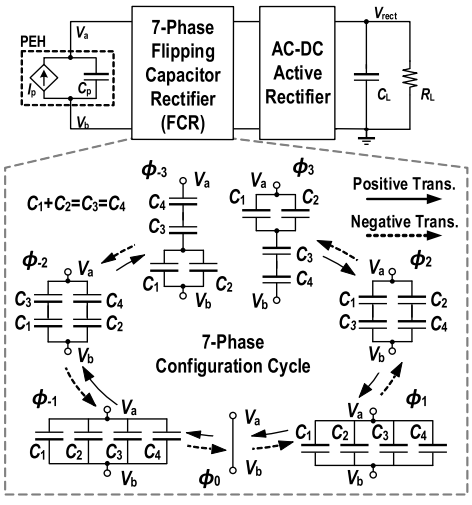


Fig. 1. System overview of the proposed 7-phase FCR piezoelectric energy harvesting interface.

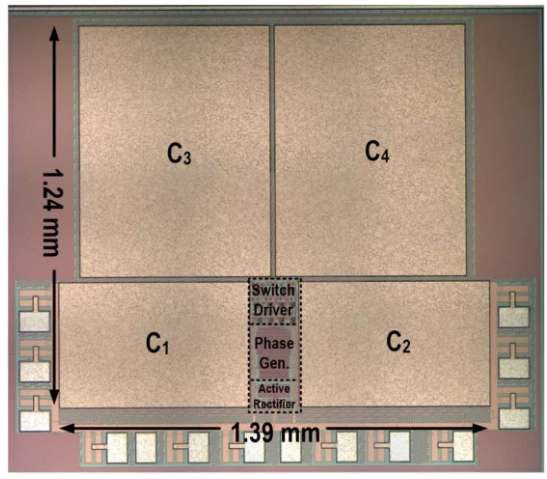


Fig. 2. Chip micrograph.

Publication(s)

[1] Z. Chen, M. K. Law, P. I. Mak, X. Zeng and R. P. Martins, "Piezoelectric Energy Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier with Capacitor-Reuse for Input Power Adaptation," IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2106-2117, Aug. 2020.

[2] Z. Chen, Y. Jiang, M.-K. Law, P.-I. Mak, X. Zeng, R. P. Martins, "A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 424-425, Feb. 2019. band TIA-Based PA Driver Achieving <-157.5dBc/Hz OB Noise" IEEE ISSCC Dig. Tech. Papers, pp. 172-174, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 4µm Diameter SPAD Using Less-doped N-Well Guard Ring in Baseline 65nm CMOS

Yang Jiang, Man-Kay Law, Pui-In Mak, Rui P. Martins

FEATURES

Small size SPAD in baseline 65nm CMOS

Low dark count @73cps/µm²@20℃

High fill factor @17.7%

High peak photon detection efficiency (PDE) @9.2%

Silicon verified in baseline 65 nm CMOS

DESCRIPTION

The work proposed a small size single photon avalanche diode (SPAD) in baseline 65nm CMOS suitable for low cost time-of-flight application with high spatial resolution. The realization in advanced CMOS process offers the possibility of reducing the footprint of in-pixel electronics. By exploiting the less-doped n-well region to surround the vertical p-well/deep-nwell multiplication region, the electric field at the SPAD periphery can be reduced without process modifications while avoiding premature lateral breakdown. Based on COMSOL simulation results, the electric field in guard ring region can be ~2× lower than that at the avalanche junction. Due to the highly doped deep n-well region, the high electric field can be restricted at the vertical p-well/deep n-well interface, achieving robust SPAD operation without premature lateral breakdown at a moderate excess bias voltage (V_{EB}).

Implemented in 65nm baseline CMOS, this work shows a measured DCR of 73cps/µm²@20℃ and V_{EB}=1V. The DCR drastically increases with V_{EB} > 2.2V due to the second breakdown at the edge, indicating the maximum V_{EB} to achieve safe SPAD operation. The PDE enhances when V_{EB} increases from 1V to 2V as a result of a larger avalanche triggering probability, with a peak of 9.2% at 480nm with V_{EB} = 2V. With a laser jitter of 80ps, the full-width half maximum (FWHM) response are 343ps, 286ps, 238ps at V_{EB} = 1V, 1.5V and 2V, respectively.

Benchmarking with the prior art, this work demonstrates a compact SPAD with a small device size and a low DCR in 65nm baseline CMOS. We can achieve a ~2.8× improvement in fill factor with a comparable device active area when compared with prior arts.

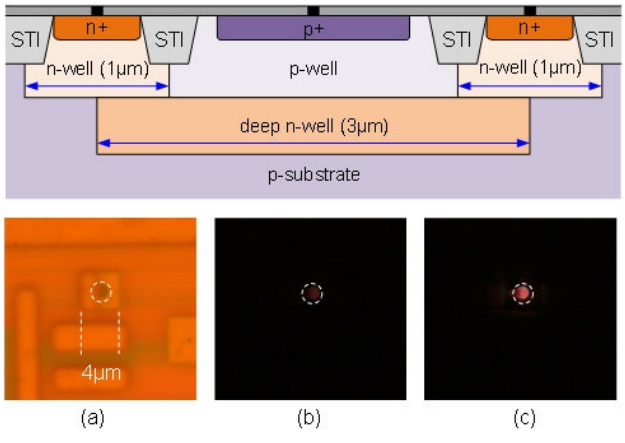


Fig. 1. Cross section of the proposed 4µm-diameter SPAD device in baseline 65nm CMOS, and (a) the chip micrograph together with the light emission test at (b) V_{EB}=1V and (c) V_{EB}=2.8V.

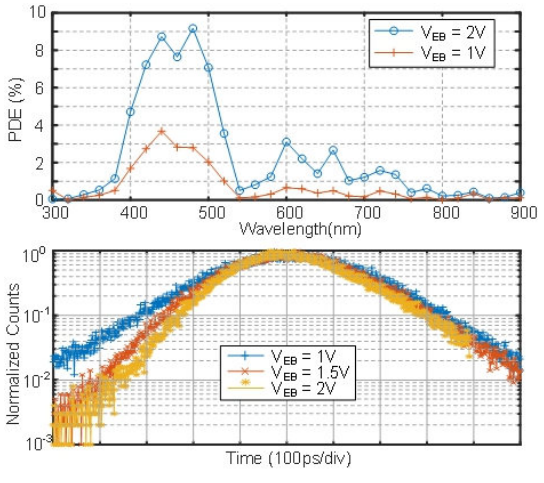


Fig. 2. Measured PDE against wavelength and timing jitter at different V_{EB}.

Publication(s)

[1] Xin Lu, Man-Kay Law, Yang Jiang, Xiaojin Zhao, Pui-In Mak and Rui P. Martins, "A 4µm Diameter SPAD Using Less-doped N-Well Guard Ring in Baseline 65nm CMOS," IEEE Transactions on Electron Devices, vol. 67, pp. 2223-2225, May 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement

Zhiyuan Chen, Yang Jiang, Man-Kay Law, Pui-In Mak, Xiaoyang Zeng, Rui P. Martins

FEATURES

Efficient energy extraction using SPFCR

Output voltage control with MVCR SC DC-DC converter

Multi-phase operation with capacitor reuse

Wide input power adaptation

MPPT with fractional $V_{OC,FBR}$ to relax sustained voltage

Silicon verified in standard 180 nm 1.8/3.3/6V CMOS

DESCRIPTION

The work proposed split-phase flipping-capacitor rectifier (SPFCR) to strategically reconfigure capacitors into a selected set of extended and augmented phases to balance between the PEH energy extraction efficiency and implementation complexity. We can remove insignificant flipping phases through phase selection to relax the system implementation complexity without sacrificing the energy harvesting efficiency. The proposed SPFCR interface with phase selection can achieve a total of 21 flipping phases using only 4 capacitors. We also propose to reconfigure the 4 capacitors into a multiple voltage conversion ratio (MVCR) switched-capacitor DC-DC converter during the non-flipping period for improving the system input power (P_{in}) adaptation without extra passives. To avoid using the boosted SPFCR open circuit voltage ($V_{OC,SPFCR}$) for maximum power point tracking (MPPT), we further demonstrate the feasibility of using the fractional FBR open circuit voltage ($V_{OC,FBR}$) instead.

Fabricated in standard 180-nm 1.8/3.3/6V CMOS, this work demonstrates the successful 21-phase SPFCR operation with a high maximum output power improving rate (MOPIR) of 9.3× (@VD=0.12V), and up to 9× over a wide $P_{in,FBR}$ input power adaptation at V_{OUT}=2V. A pseudo-constant relationship between between $V_{mpp,SPFCR}$ and $2V_{OC,FBR}$ at different input power is also reported for MPPT operation.

Benchmarking with the prior art, this work achieves 21-phase operation using only 4 capacitors, and demonstrates a wide input power adaptation using the proposed capacitor-reuse MVCR SC DC-DC converter approach. Without using an excessively large external high Q inductor in the order of mH, this work reports a PEH interface that exhibits a high MOPIR with output voltage control and relaxed voltage tolerance requirement.

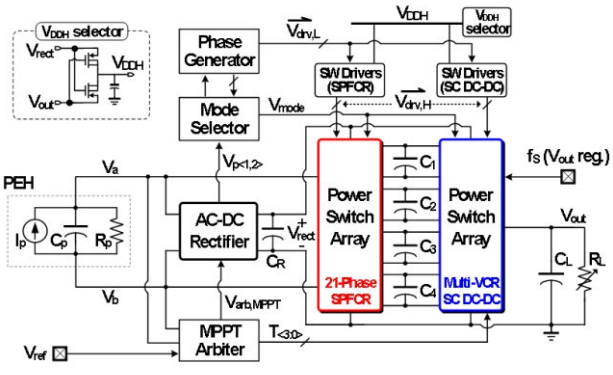


Fig. 1. System overview of the proposed SPFCR and capacitor reuse multiple-VCR SC DC-DC converter for piezoelectric energy harvesting.

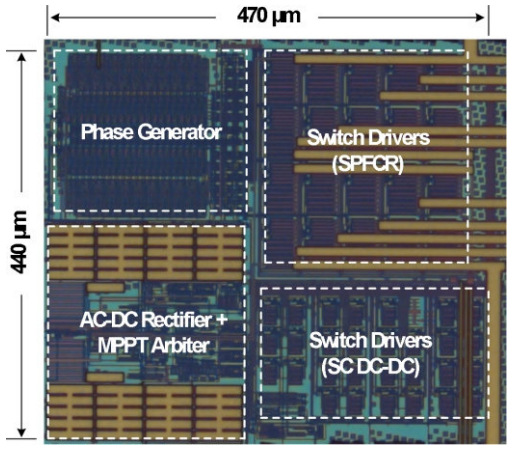


Fig. 2. Chip micrograph.

Publication(s)

[1] Z. Chen, M. K. Law, P. I. Mak, X. Zeng and R. P. Martins, "Piezoelectric Energy Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier with Capacitor-Reuse for Input Power Adaptation," IEEE Journal of Solid-State Circuits, vol. 55, no. 8, pp. 2106-2117, Aug. 2020.

[2] Z. Chen, Y. Jiang, M.-K. Law, P.-I. Mak, X. Zeng, R. P. Martins, "A Piezoelectric Energy-Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier (FCR) and Capacitor Reuse Multiple-VCR SC DC-DC Achieving 9.3x Energy-Extraction Improvement," IEEE International Solid-State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 424-425, Feb. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes for Biomedical Implant Applications

Zhiyuan Chen, Man-Kay Law, Pui-In Mak, Rui P. Martins

FEATURES

Ultra-compact single chip solution for implants

High efficiency on-chip solar energy harvesting

Parallel photodiode configurations

PDSC for startup time improvement

Systematic charge pump/solar cell area optimization

Silicon verified in standard 180 nm CMOS

DESCRIPTION

The work proposed an ultra-compact single-chip solar energy harvesting IC using on-chip solar cell for biomedical implant applications. By employing an on-chip charge pump with parallel connected photodiodes, a significant efficiency improvement can be achieved when compared with the conventional stacked photodiode approach to boost the harvested voltage while preserving a single-chip solution. A photodiode-assisted dual startup circuit (PDSC) is also proposed to improve the area efficiency and increase the system startup speed. By employing an auxiliary charge pump (AQP) using zero threshold voltage (ZVT) devices in parallel with the main charge pump, a low startup voltage of 0.25 V is obtained while minimizing the reversion loss. A 4Vin gate drive voltage is utilized to reduce the conduction loss. Systematic charge pump and solar cell area optimization is also introduced to improve the energy harvesting efficiency.

Fabricated in standard 180-nm 1.8/3.3/6V CMOS, this work occupies an active area of 1.54 mm^2. Measurement results show that the on-chip charge pump can achieve a maximum efficiency of 67%. With an incident power of 1.22 mW/cm^2 from a halogen light source, the proposed energy harvesting IC can deliver an output power of 1.65 µW at 64% charge pump efficiency.

Benchmarking with the prior art, the on-chip charge pump achieves the highest efficiency at low incident power levels (with an input voltage close to 0.3 V) which is expected in subdermal implant applications. Among existing single-chip solar energy harvesting solutions, this work demonstrates the highest energy harvesting efficiency (~3.5× improvement while generating a boosted output voltage for system use.

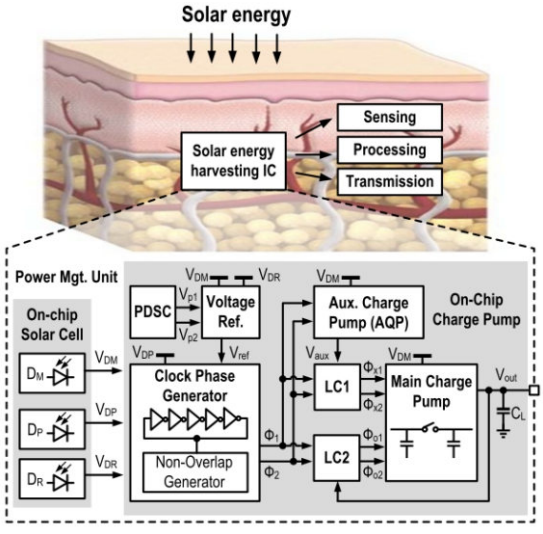


Fig. 1. System overview of the proposed single -chip solar energy harvesting IC.

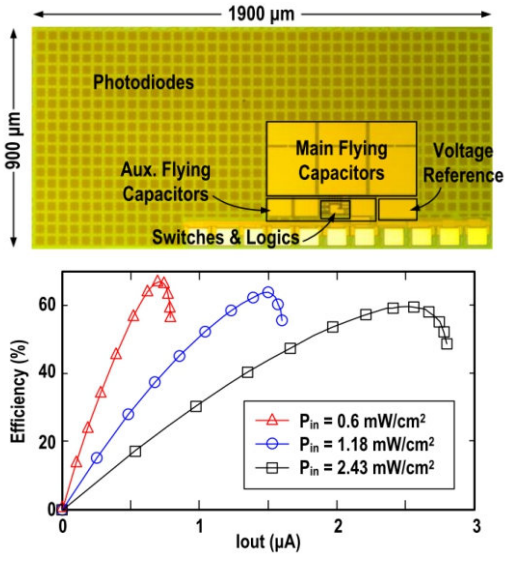


Fig. 2. Chip micrograph and measured efficiency under different incident power levels.

Publication(s)

[1] Z. Chen, M. K. Law, P. I. Mak and R. P. Martins, "A Single-Chip Solar Energy Harvesting IC using Integrated Photodiodes with a 67% Charge Pump Maximum Efficiency," IEEE Transactions on Biomedical Circuits and Systems, vol. 11, no. 1, pp. 44-53, Feb. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter with Wide Input Voltage Range and Enhanced Power Density

Yang Jiang, Man-Kay Law, Zhiyuan Chen, Pui-In Mak, Rui P. Martins

FEATURES

Systematic algebraic series-parallel topology for flexible rational VCR generation

Efficient fully integrated SC DC-DC boost conversion

Optimal conduction loss

Reduced parasitic loss

Silicon verified in standard 180 nm CMOS

DESCRIPTION

The work proposed an algebraic series-parallel (ASP) topology for fully integrated switched-capacitor (SC) DC-DC boost converters with flexible fractional voltage conversion ratios (VCRs). By elaborating the output voltage (VOUT) expression into a specific algebraic form, the proposed ASP can achieve improvements on both the charge sharing and bottom-plate-parasitic losses while maintaining the high topology and fractional VCR flexibility of conventional two-dimensional series-parallel (2DSP) converters. The proposed method consists of a generic ASP topology framework with systematic parameter determination for precise converter implementation, and can theoretically surpass the power conversion efficiency (PCE) of 2DSP converters.

Fabricated in 65nm bulk CMOS, we designed a fully integrated ASP-based SC rational boost converter by cascading with the Dickson topology, with a total of 7 rational VCRs to boost an input voltage of 0.25-to-1V to a 1V output. Delivering a maximum loading power of 20.4mW, the chip prototype achieves a peak efficiency of 80% at a power density of 22.7mW/mm².

Benchmarking with the prior art, this work with the other fully integrated SC boost converters, in both bulk CMOS and special processes. It can be observed that this work exhibits a higher power density while achieving a high number of VCR when compared with the existing designs in bulk CMOS.

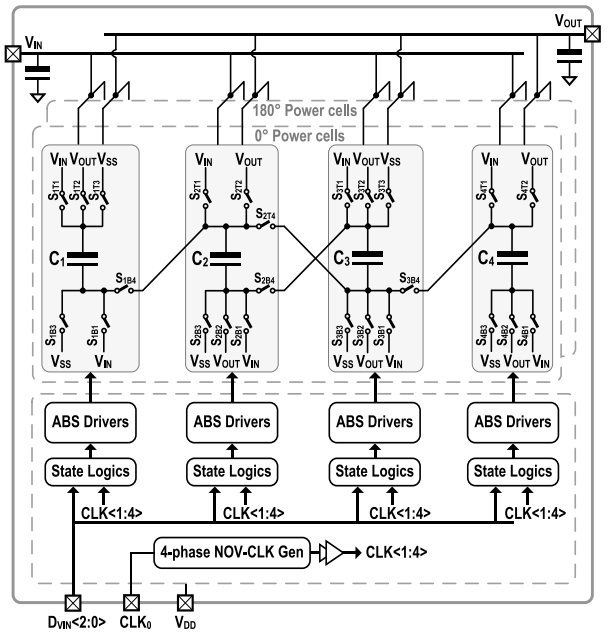


Fig. 1. System overview of the implemented ASP SC boost converter.

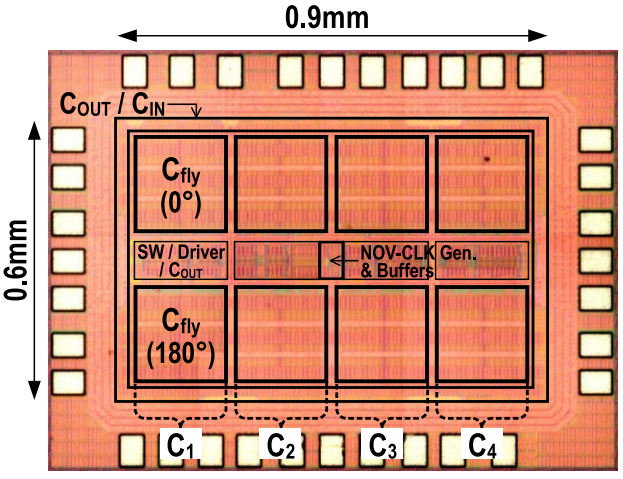


Fig. 2. Chip micrograph.

Publication(s)

[1] Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density," IEEE Journal of Solid-State Circuits, vol. 54, no. 11, pp. 3118-3134, Nov. 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS

Lab-on-a-Chip

Hydrodynamic-Flow-Enhanced Rapid Mixer for Isothermal DNA Hybridization Kinetics Analysis on Digital Microfluidics Platform -------- 80

A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips -------- 81

A digital microfluidic system for loop-mediated isothermal Amplification and sequence specifc pathogen detection -------- 82

A digital microfluidic system with 3D microstructures for single-cell culture -------- 83

Clip-to-release on amplification (CRoA): a novel DNA amplificationenhancer on and off microfluidics -------- 84

Drug screening of cancer cell lines and human primary tumors using droplet microfluidics -------- 85

Turning on/off satellite droplet ejection for flexible sampledelivery on digital microfluidics -------- 86

Hydrodynamic-Flow-Enhanced Rapid Mixer for Isothermal DNA Hybridization Kinetics Analysis on Digital Microfluidics Platform

Mingzhong Li, Cheng Dong, Man-Kay Law, Yanwei Jia, Pui-In Mak, Rui P. Martins

FEATURES

Automated isothermal DNA hybridization kinetics on complete DMF platform

Stable droplet temperature (within ±0.1oC)

Rapid mixer with slow frequency AC actuation

Faster reaction rate than pure diffusion (>13×)

DESCRIPTION

This paper presents a DMF platform that can perform isothermal hydrodynamic-flow-enhanced droplet mixing to enhance the hybridization efficiency while ensuring a stable droplet temperature (within ±0.1℃). Specifically, with a single electrode, droplet-boundary oscillation under a slow AC actuation is studied for improving the reaction rate. The dependencies between the mixing efficiency and the actuation voltage, actuation frequency and the spacer thickness are also systematically studied. Reliable mixing efficiency improvement is further validated over a wide range of solute concentrations. The results from real-time on-chip DNA hybridization kinetics with stationary droplets using the complete sandwiched DMF system shows that the proposed rapid mixer can achieve the same hybridization equilibrium with >13 times faster reaction rate when compared to the reference one through pure diffusion, while preventing biased hybridization kinetics as demonstrated in the electrothermal technique.

Benefitting from the mechanical mixing process, the proposed method can achieve efficient mixing independently of the solute concentrations for flexible hybridization experiments. The negligible temperature change is also favourable for the discrimination of matched and mismatched binding for the DNA hybridization kinetics investigation.

Based on the hybridization experiments of Kras gene and its corresponding molecular beacon probe in a complete DMF platform, the hybridization equilibrium is more readily and accurately achieved with the proposed micro-mixing technique over the diffusion and the electrothermal counterparts on DMF platform.

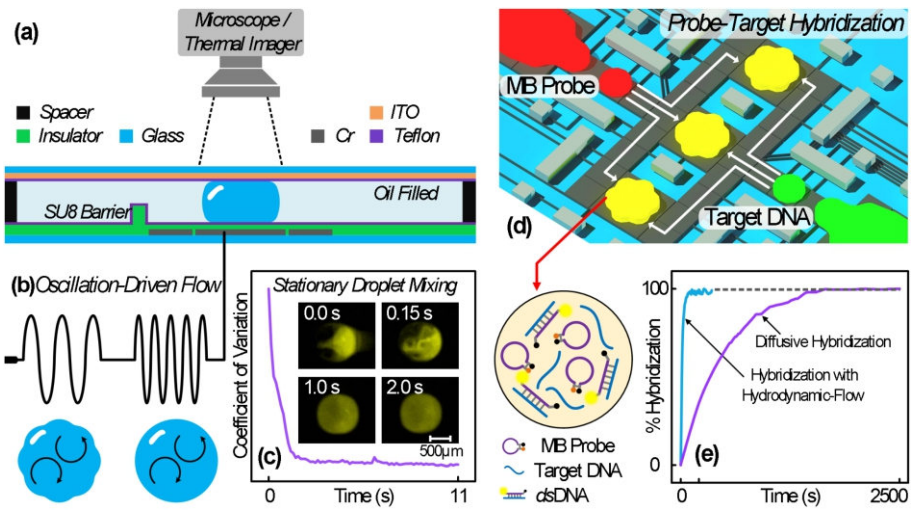


Fig. 1. (a) Sandwiched DMF device monitored by fluorescence microscope and thermal imager. (b) Droplet oscillation patterns and internal hydrodynamic flow at sub-kHz actuation frequency. (c) Stationary droplet mixing with 1-μM fluorophore DNA probe and 10-mM Tris-HCl buffer. (d) SE isometric view with the molecular beacon probe and target DNA dispensed and driven to the reaction chambers. (e) Real-time DNA hybridization kinetics through fluorescence with passive diffusion and the proposed hydrodynamic-flow enhancement method.

Publication(s)

[1] M. Li, C. Dong, M. K. Law, Y. Jia, P. I. Mak and R. P. Martins, “Hydrodynamic-flow-enhanced rapid mixer for isothermal DNA hybridization kinetics analysis on digital microfluidics platform,” Sensors and Actuators B: Chemical, vol. 287, pp. 390-397, May 2019.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips

Cheng Dong, Yanwei Jia, Jie Gao, Tianlan Chen, Pui-In Mak and Rui P. Martins

FEATURES

3D microstructures on DMF chip

Multiple droplet splitting in one step

Parallel DNA analysis on-chip

DESCRIPTION

Existing digital microfluidic (DMF) chips exploit the electrowetting on dielectric (EWOD) force to perform droplet splitting. However, the current splitting methods are not flexible and the volume of the droplets suffers from a large variation. Herein, we propose a DMF chip featuring a 3D microblade structure to enhance the droplet-splitting performance. By exploiting the EWOD force for shaping and manipulating the mother droplet, we obtain an average dividing error of <2% in the volume of the daughter droplets for a number of fluids such as deionized water, DNA solutions and DNA–protein mixtures. Customized droplet splitting ratios of up to 20 : 80 are achieved by positioning the blade at the appropriate position. Additionally, by fabricating multiple 3D microblades on one electrode, two to five uniform daughter droplets can be generated simultaneously. Finally, by taking synthetic DNA targets and their corresponding molecular beacon probes as a model system, multiple potential pathogens that cause sepsis are detected rapidly on the 3D-blade-equipped DMF chip, rendering it as a promising tool for parallel diagnosis of diseases.

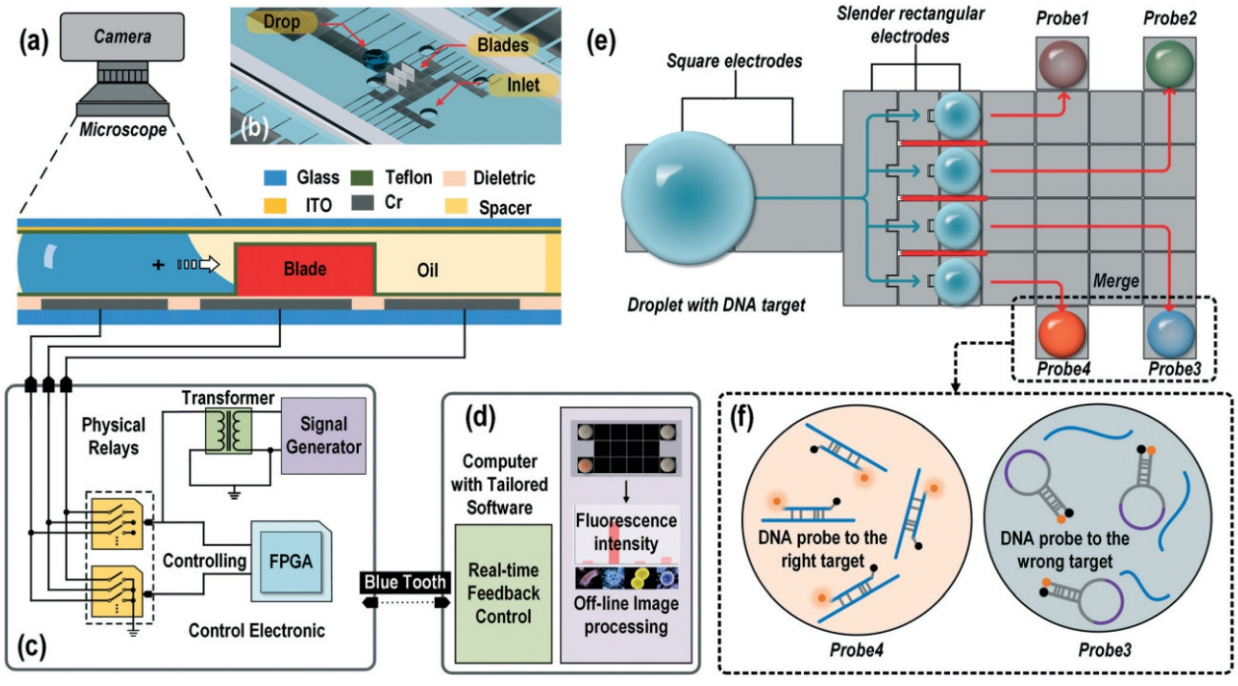


Fig. 1. Digital microfluidic device embedded with on-chip 3D blades for precise quantitative droplet splitting

Publication(s)

[1] C. Dong, Y. W. Jia, J. Gao, T. L. Chen, P. I. Mak, M. I. Vai and R. P. Martins, A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips, Lab on a Chip, 17, 896-904, 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A digital microfluidic system for loop-mediated isothermal Amplification and sequence specifc pathogen detection

Liang Wan, Tianlan Chen, Jie Gao, Cheng Dong, Ada Hang-Heng Wong, Yanwei Jia, Pui-In Mak, Chu-Xia Deng, Rui Martins

FEATURES

Isothermal DNA amplification on digital microfluidics

Specific DNA detection

No false positive DNA detection

DESCRIPTION

A digital microfluidic (DMF) system has been developed for loop-mediated isothermal amplification (LAMP)-based pathogen nucleic acid detection using specifc low melting temperature (Tm) Molecular Beacon DNA probes. A positive-temperature-coefcient heater with a temperature sensor for real-time thermal regulation was integrated into the control unit, which generated actuation signals for droplet manipulation. To enhance the specifcity of the LAMP reaction, low-Tm Molecular Beacon probes were designed within the single-stranded loop structures on the LAMP reaction products. In the experiments, only 1 µL of LAMP reaction samples containing purifed Trypanosoma brucei DNA were required, which represented over a 10x reduction of reagent consumption when comparing with the conventional off-chip LAMP. On-chip LAMP for unknown sample detection could be accomplished in 40 min with a detection limit of 10 copies/reaction. Also, we accomplished an on-chip melting curve analysis of the Molecular Beacon probe from 30 to 75 °C within 5 min, which was 3x faster than using a commercial qPCR machine. Discrimination of non-specifc amplifcation and lower risk of aerosol contamination for on-chip LAMP also highlight the potential utilization of this system in clinical applications. The entire platform is open for further integration with sample preparation and fluorescence detection towards a total-micro-analysis system

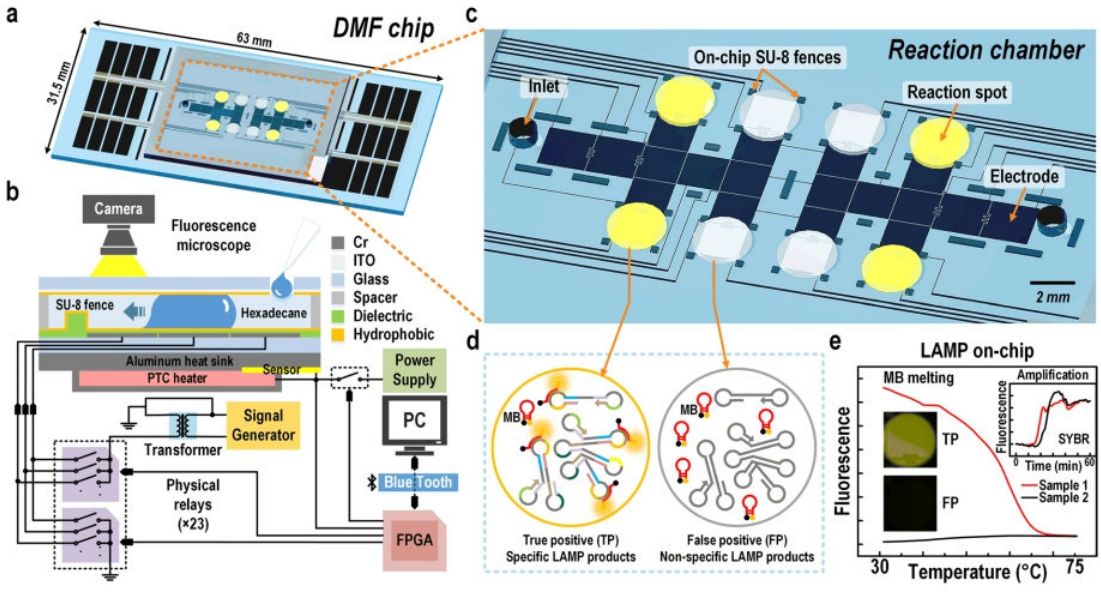


Fig. 1. Overview of the digital microfluidic system for loop-mediated isothermal amplification (LAMP) reaction and melting curve analysis using Molecular Beacon DNA probes.

Publication(s)

[1] L. Wan, T. L. Chen, J. Gao, C. Dong, A. H. H. Wong, Y. W. Jia*, P. I. Mak, C. X. Deng and R. Martins, A digital microfluidic system for loop-mediated isothermal amplification and sequence specific pathogen detection, Scientific Reports, 7, 14586, 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A digital microfluidic system with 3D microstructures for single-cell culture

Jiao Zhai, Haoran Li, Ada Hang-Heng Wong, Cheng Dong, Shuhong Yi, Yanwei Jia, Pui-In Mak, Chu-Xia Deng, Rui P. Martins

FEATURES

3D microstructures on digital microfluidic chip
Low voltage for drop actuation
Single cell drug screening
No evaporation of drop on-chip

DESCRIPTION

Despite the precise controllability of droplet samples in digital microfluidic (DMF) systems, their capability in isolating single cells for long-time culture is still limited: typically, only a few cells can be captured on an electrode. Although fabricating small-sized hydrophilic micropatches on an electrode aids single-cell capture, the actuation voltage for droplet transportation has to be significantly raised, resulting in a shorter lifetime for the DMF chip and a larger risk of damaging the cells. In this work, a DMF system with 3D microstructures engineered on-chip is proposed to form semiclosed micro-wells for efficient single-cell isolation and long-time culture. Our optimum results showed that approximately 20% of the micro-wells over a 30 × 30 array were occupied by isolated single cells. In addition, lowevaporation-temperature oil and surfactant aided the system in chieving a low droplet actuation voltage of 36V, which was 4 times lower than the typical 150 V, minimizing the potential damage to the cells in the droplets and to the DMF chip. To exemplify the technological advances, drug sensitivity tests were run in our DMF system to investigate the cell response of breast cancer cells (MDA-MB-231) and breast normal cells (MCF-10A) to a widely used chemotherapeutic drug, Cisplatin (Cis). The results on-chip were consistent with those screened in conventional 96-well plates. This novel, simple and robust single-cell trapping method has great potential in biological research at the single cell level.

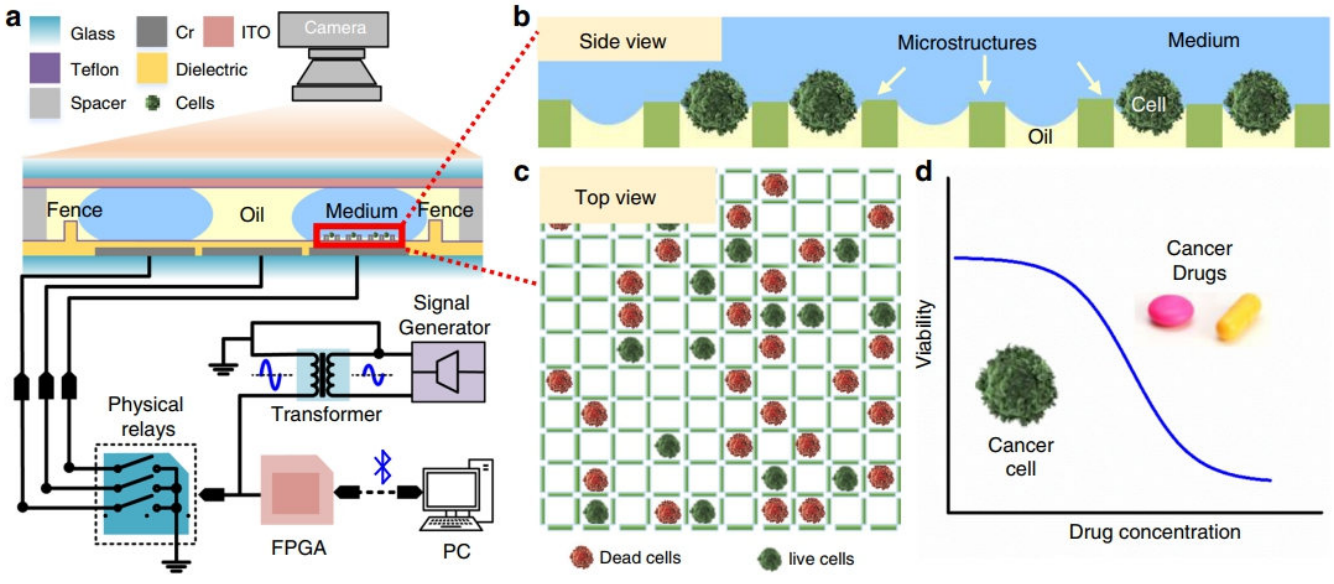


Fig. 1. Schematic of the digital microfluidic system for single cell culture and drug toxicity tests

Publication(s)

[1] J. Zhai, H. R. Li, A. H. H. Wong, C. Dong, S. H. Yi, Y. W. Jia*, P. I. Mak, C. X. Deng and R. P. Martins, A digital microfluidic system with 3D microstructures for single-cell culture, Microsystems and Nanoengineering, 6, 6, 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Clip-to-release on amplification (CRoA): a novel DNA amplification enhancer on and off microfluidics

Ren Shen, Yanwei Jia, Pui-In Mak and Rui P. Martins

FEATURES

Novel reagent for DNA amplification on/off microfluidics

10 x brighter amplification signal

No false negative results

DESCRIPTION

Despite its high sensitivity, low cost, and high efficiency as a DNA amplification indicator with a yes/no answer, dsDNA-binding dye encounters incompatibility when used in microfluidic systems, resulting in problems such as false negative amplification results. Besides, its inhibition of amplification at high concentrations hinders its application both on-chip and off-chip. In this study, we propose a novel DNA amplification enhancer to counteract the drawbacks of dsDNA-binding dyes. It acts as a temporary reservoir for the free-floating dyes in solution and releases them on demand during the amplification process. Through this clip-to-release on amplification mechanism, the enhancer lowered the background fluorescence of sample droplets before amplification, enhanced the signal-to-background ratio of positive samples, and eliminated the false negative signal of on-chip PCR. Moreover, the enhancer increased the off-chip polymerase chain reaction (PCR) efficiency, boosted the fluorescence signal up to 10-fold, and made less nonspecific amplification product. All the factors affecting the enhancer's performance are investigated in detail, including its structure and concentration, and the types of dsDNA-binding dye used in the reaction. Finally, we demonstrated the broad application of the proposed amplification enhancer in various DNA amplification systems, for various genes, and on various amplification platforms. It would reignite the utilization of dsDNA dyes for wider applications in DNA analysis both on-chip and off-chip.

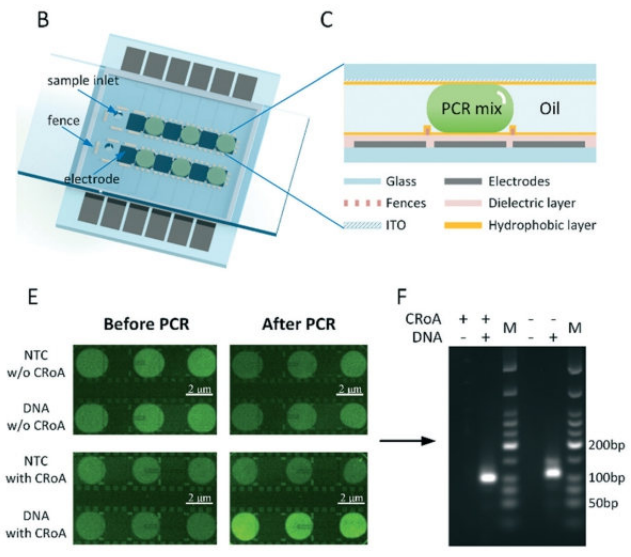


Fig. 1. proof of principle experiments of the CRoA PCR enhancing function for on-chip PCR.

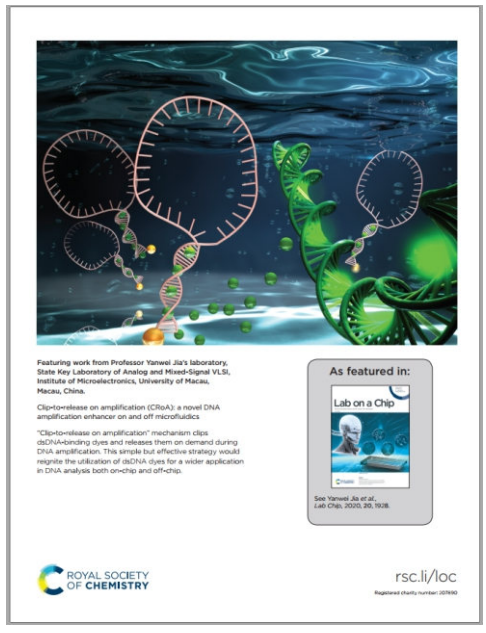


Fig. 2. Back Cover featured story in Lab on a Chip.

Publication(s)

[1] R. Shen, Y. W. Jia*, P. I. Mak, and R. P. Martins, Clip to release on amplification (CRoA): a novel enhancer for DNA amplification on and off microfluidics, Lab on a Chip, 20, 1928-1938, 2020 (Outside Back Cover).

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Drug screening of cancer cell lines and human primary tumors using droplet microfluidics

Ada Hang-Heng Wong, Haoran Li, Yanwei Jia, Pui-In Mak, Rui P. Martins, Yan Liu, Chi Man Vong, Hang Cheong Wong, Pak Kin Wong, Haitao Wang, Heng Sun, Chu-Xia Deng

FEATURES

Droplet microfluidics
High throughput multiple drug screening on-chip
Primary tumor drug screening
Precision medicine

DESCRIPTION

Precision Medicine in Oncology requires tailoring of therapeutic strategies to individual cancer patients. Due to the limited quantity of tumor samples, this proves to be difcult, especially for early stage cancer patients whose tumors are small. In this study, we exploited a 2.4 ×2.4 centimeters polydimethylsiloxane (PDMS) based microfluidic chip which employed droplet microfluidics to conduct drug screens against suspended and adherent cancer cell lines, as well as cells dissociated from primary tumor of human patients. Single cells were dispersed in aqueous droplets and imaged within 24 hours of drug treatment to assess cell viability by ethidium homodimer 1 staining. Our results showed that 5 conditions could be screened for every 80,000 cells in one channel on our chip under current circumstances. Additionally, screening conditions have been adapted to both suspended and adherent cancer cells, giving versatility to potentially all types of cancers. Hence, this study provides a powerful tool for rapid, low-input drug screening of primary cancers within 24 hours after tumor resection from cancer patients. This paves the way for further technological advancement to cutting down sample size and increasing drug screening throughput in advent to personalized cancer therapy.

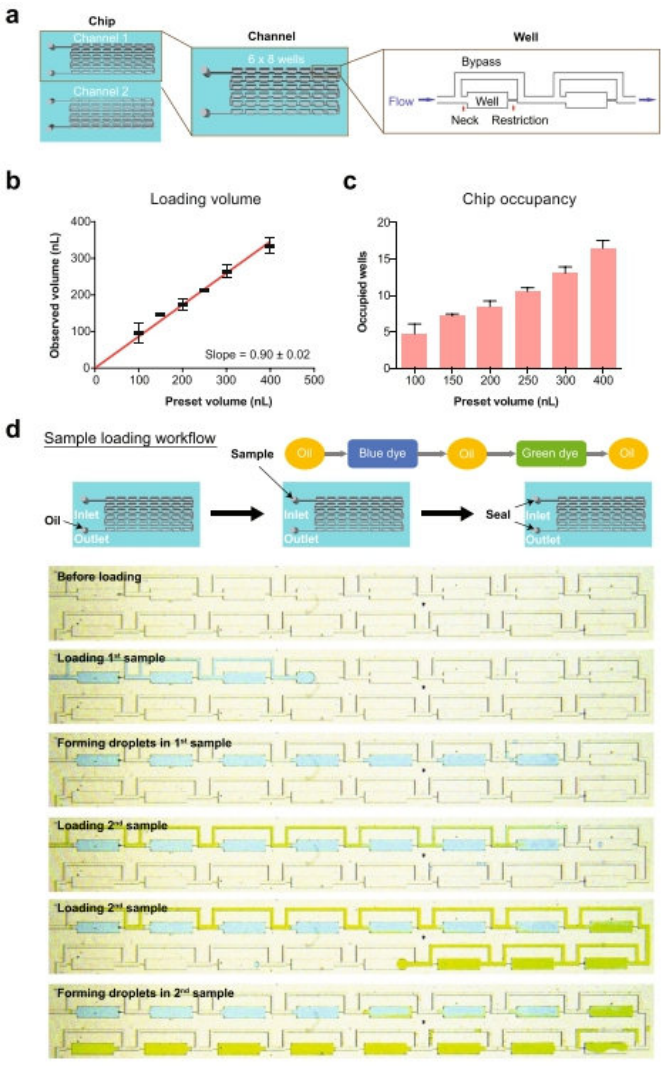


Fig. 1. Microfluidic chip design and validation

Publication(s)

[1] A. H. H. Wong, H. R. Li, Y. W. Jia, P. I. Mak, R. P. Martins, Y. Liu, C. M. Vong, H. C. Won, P. K. Wong, H. T. Wang, H. Sun, C. X. Deng, Drug screening of cancer cell lines and human primary tumors using droplet microfluidics, Scientific Reports, 7, 9109, 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Turning on/off satellite droplet ejection for flexible sample delivery on digital microfluidics

Haoran Li, Ren Shen, Cheng Dong, Tianlan Chen, Yanwei Jia, Pui-In Mak and Rui P. Martins

FEATURES

Sample delivery on digital microfluidic chip

Easy electric controlled sample delivery

Wide range from pL to nL

DESCRIPTION

Digital microfluidics has the potential to minimize and automate reactions in biochemical labs. However, the complexity of drop manipulation and sample preparation on-chip has limited its incorporation into daily workflow. In this paper, we report a novel method for flexible sample delivery on digital microfluidics in a wide volume range spanning four orders of magnitude from picoliters to nanoliters. The method is based on the phenomenon of satellite droplet ejection, triggered by a sudden change in the strength of the electric field across a drop on a hydrophobic dielectric surface. By precisely modulating the actuation signal with convenient external electric controls, satellite droplet ejection can be turned on to dispense samples or turned off to transport picking-up drops. A pico-dosing design is presented and validated in this work to demonstrate the direct and flexible on-chip sample delivery. This approach could pave the way for the acceptance of microfluidics as a common platform for daily reactions to realize lab-on-a-chip.

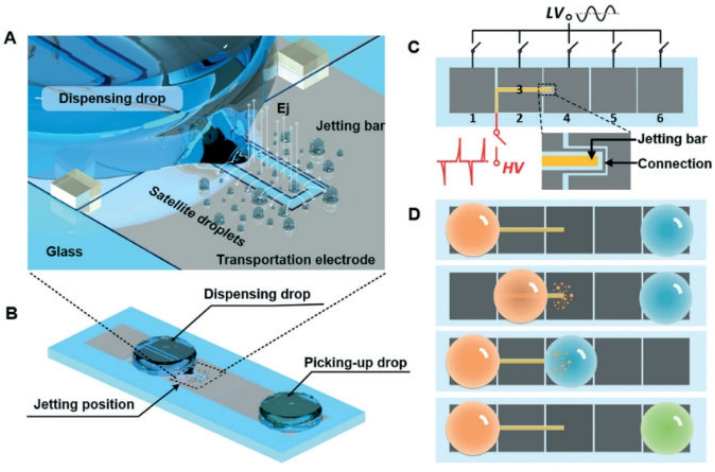


Fig. 1. Design of the pico-dosing technique on digital microfluidics

Fig. 2. Front Cover featured story in Lab on a Chip.

Publication(s)

[1] H. R. Li, R. Shen, Y. W. Jia*, P. I. Mak, R. P. Martins, Turning on/off satellite droplet ejection for flexible sample delivery on digital microfluidics, Lab on a Chip, 20,3709-3719, 2020 (Inside Front Cover).

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

RESEARCH ABSTRACTS

Power Management and Conditioning Circuits

A 0.5-V supply, 36nW bandgap reference with 42ppm/°C average temperature coefficient within -40°C to 120°C -------- 88

A 220-MHz Bondwire-Based Fully-Integrated KY Converter with Fast Transient Response under DCM Operation -------- 89

A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Selection for IoT Application -------- 90

A Deadbeat Current Controller of LC-Hybrid Active Power Filter for Power Quality Improvement -------- 91

A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery -------- 92

A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging -------- 93

Adaptive Thyristor Controlled LC – HAPF for Reactive Power and Current Harmonics Compensation with Switching Loss Reduction -------- 94

Analysis, Control and Design of Hybrid Grid-Connected Inverter for Renewable Energy Generation with Power Quality Conditioning -------- 95

Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter -------- 96

Effects of Parasitic Resistances on Magnetically Coupled Impedance-Source Networks -------- 97

A Hybrid Boost Converter With Cross-Connected Flying Capacitors -------- 98

An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction -------- 99

An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery -------- 100

A Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Display -------- 101

A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation -------- 102

A VHF Wide-Input Range CMOS Passive Rectifier with Active Bias Tuning -------- 103

An NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28-nm CMOS -------- 104

A 0.5-V supply, 36nW bandgap reference with 42ppm/°C average temperature coefficient within -40°C to 120°C

Chi-Wa U, Wen-Liang Zeng, Man-Kay Law, Chi-Seng Lam, and Rui P. Martins

FEATURES

Low supply voltage (0.5V)

Low power consumption (36 nW)

Wide Operating temperature range (-40 – 120°C)

Switched capacitor circuits

Silicon verified in TSMC 65 nm CMOS

DESCRIPTION

This work presents a switched capacitor network (SCN)-based bandgap voltage reference (BGR) circuit with a wide temperature range, high precision, low supply voltage and low power consumption, which is suitable for IoT device application. The proposed BGR employs a 2x charge pump (CP) with an adjusted capacitor ratio to minimize the ripple to supply the V_{EB} generator, which can relax V_{DD} from 0.9V to 0.5V.A proportional to absolute temperature (PTAT) current source is proposed to bias the PNP BJT in order to reduce the nonlinearity of V_{EB}, thus improving the TC and extending the temperature range of the BGR. Moreover, a voltage divider SCN with low leakage consideration to form the complementary to absolute temperature (CTAT) voltage is designed to reduce the nonlinearity of its coefficient thus benefit for improving the TC and extending the temperature range, while a series-parallel SCN with adjusted clock swing to form the PTAT voltage is designed to improve the line regulation of the BGR. Also, four kinds of second-order effect that affect the TC of the coefficient of CTAT and PTAT voltage are studied. According to the analysis and simulation result, it can be eliminated during the design process.

The proposed SCN-based BGR was implemented in a 65nm process and occupied a chip area of 0.18 × 0.29 mm², which has an average temperature coefficient (TC) of 42 ppm/°C at 0.5V supply within − 40 °C to 120 °C. The line regulation is 3.2mV/V or 0.64%/V from 0.5V to 1V. Based on 6-chip test result, it shows a 3σ /μ variation of 3.08% before trimming, while 0.36% after trimming.

Benchmarking with the prior art, this work succeeds in extending the operating temperature range of the BJT-based BGR under a low supply voltage as well as achieved a small TC while remains a small power consumption.

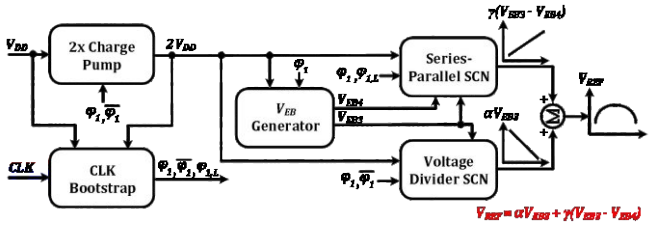


Fig. 1. Architecture of proposed BGR circuit

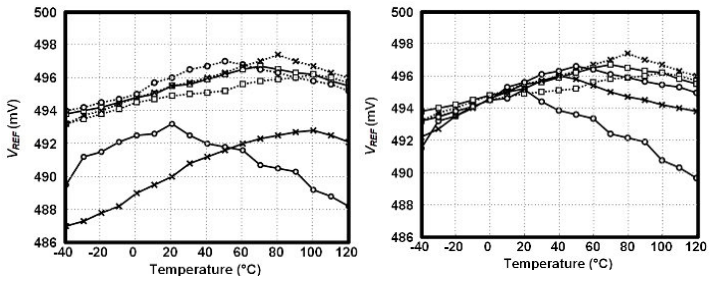


Fig. 2. The measured (a) untrimmed, (b) trimmed V_{REF} from -40 to 120 °C.

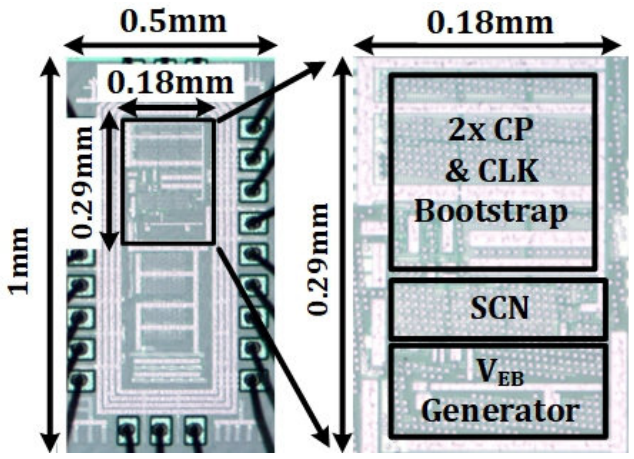


Fig. 3. Chip micrograph.

Publication(s)

[1] C.-W. U, W.-L. Zeng, M.-K. Law, C.-S. Lam, R. P. Martins, “A 0.5-V supply, 36nW bandgap reference with 42ppm/°C average temperature coefficient within -40°C to 120°C,” IEEE Transactions on Circuits and Systems I - Regular Papers, vol. 67, no. 11, pp. 3656 – 3669, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A 220-MHz Bondwire-Based Fully-Integrated KY Converter with Fast Transient Response under DCM Operation

Wen-Liang Zeng, Chi-Seng Lam, Sai-Weng Sin, Franco Maloberti, Man-Chung Wong, and Rui P. Martins

FEATURES

Fully integrated, bond-wire inductor

Hybrid DC-DC converter topology (KY converter)

High efficiency and fast transient response

Silicon verified in ST 65 nm CMOS

DESCRIPTION

This design is a 220 MHz PWM fully integrated KY DC-DC step-up converter utilizing bondwire as power inductor, with discontinuous conduction mode (DCM) calibration control as shown in Fig. 1. This is the first DCM closed-loop PWM controller for the KY converter, including 1) its parameter design; 2) a DCM resulting in large voltage ripple and Right-Half-Plane Zero (RHPZ) in the power stage transfer function. KY converter comprises a switched-capacitor charge pump converter and a buck converter, and combines the advantages of both converters and exhibits the characteristics of non-pulsating output current, low output voltage ripple and no RHPZ.

Fabricated in 65-nm CMOS, the designed KY converter core occupies 0.93 mm² (shown in Fig. 2) and achieves an output conversion range of 1.5 V to 2.0 V from a 1.2 V input. The measured peak efficiency is 75.2 %@97.5 mW as shown in Fig. 3. With a 500 ps rising/falling time of the load current step (56 mA), the undershoot/overshoot is 245/205 mV at 146/140 ns recovery time, which is competitive with the state-of-the-art boost converters.

This work succeeds in developing the KY converter in integrated circuit design, which has great potential in IoT applications.

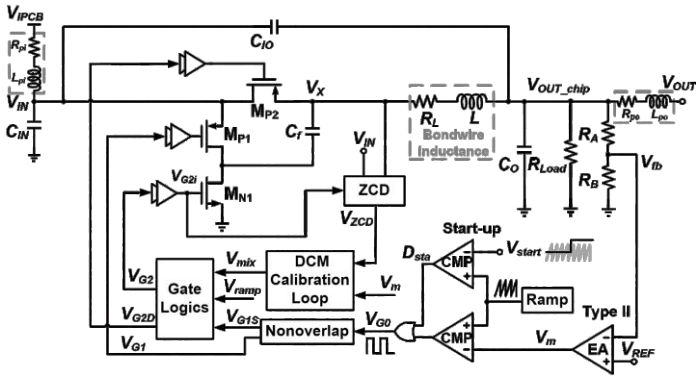


Fig. 1. System block diagram of the proposed fully integrated KY converter under DCM operation.

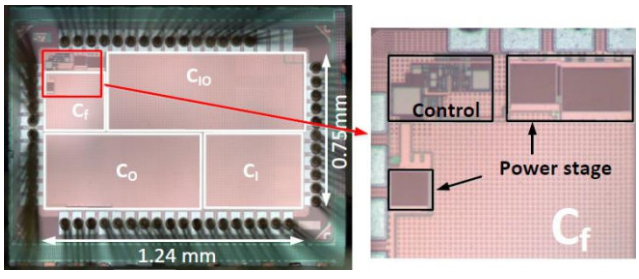


Fig. 2. Chip micrograph.

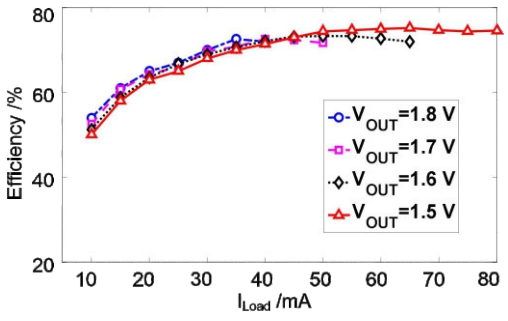


Fig. 3. Measurement power efficiency of the proposed KY converter for V_{IN} = 1.2 V and V_{OUT} = 1.5, 1.6, 1.7, 1.8 V under different load current.

Publication(s)

[1] W.-L. Zeng, C.-S. Lam, S.-W. Sin, F. Maloberti, M.-C. Wong, R. P. Martins, "A 220-MHz Bondwire-Based Fully-Integrated KY Converter with Fast Transient Response under DCM Operation", IEEE Transactions on Circuits and Systems I - Regular Papers, vol. 65, no. 11, pp. 3984 – 3995, Nov. 2018.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Selection for IoT Application

Wen-Liang Zeng, Yuan Ren, Chi-Seng Lam, Sai-Weng Sin, Weng-Keong Che, Ran Ding, and Rui P. Martins

FEATURES

Low power consumption, 470 nA quiescent current

High efficiency, 92.7%/94.7%

Wide input voltage range from 2 V to 5 V

Wide load current range from 10 µA to 50 mA

2 control modes (DCT+PWM)

Silicon verified in SMIC 180 nm CMOS

DESCRIPTION

An ultra-low quiescent current dual-mode buck converter system is designed for IoT application, which includes a double clock time (DCT) and a pulse-width-modulation (PWM) control modes as shown in Fig. 1(a). The proposed DCT mode can reduce the conversion loss over a wide loading range from nA-to-mA and achieve seamless mode transition from DCT to PWM control. This converter achieves a peak efficiency of 92.7%/94.7% in DCT/ PWM and >80% efficiency from 10 µA to 50 mA (5000x), with a wide input voltage from 2 V to 5 V as shown in Fig. 1(b). A quiescent current of 470 nA including bandgap voltage reference and internal oscillator is achieved. The DCT-to-PWM mode selection mechanism achieves an undershoot of 80 mV at 11 µs recovery time when load current jumps from 6.67 µA to 50 mA.

The prototype is fabricated in a 0.18µm CMOS with 5 V thick oxide option, and the active area is 1x1.1 mm² with PAD-ring included, as shown in Fig. 2. Due to the proposed DCT control mode and low power DCT-to-PWM mode selection circuit, the converter achieves an I_q = 470 nA at V_{IN} = 2.0 V and V_{OUT} = 0.8 V.

This work achieves a comparable I_q and efficiency with the state-of-the-art DC-DC converters and similar product.

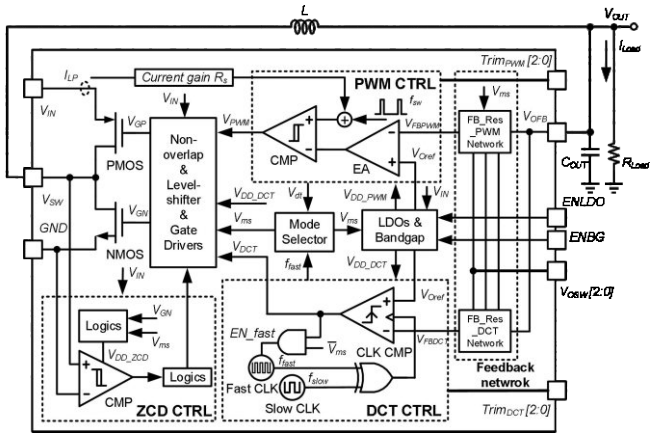


Fig. 1. System block diagram of the proposed DCT/PWM buck converter.

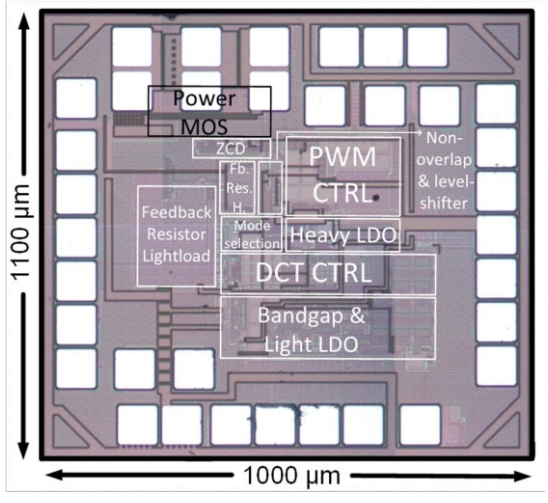


Fig. 2. Chip micrograph.

Publication(s)

[1] W.-L. Zeng, Y. Ren, C.-S. Lam, S.-W. Sin, W.-K. Che, R. Ding, R. P. Martins, "A 470nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter with Seamless Mode Transition for IoT Application", IEEE Transactions on Circuits and Systems I - Regular Papers, vol. 67, no. 11, pp. 4085 – 4098, Nov. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Allwinner Technology Co., Ltd.

A Deadbeat Current Controller of LC-Hybrid Active Power Filter for Power Quality Improvement

Wai-Kit Sou, Wai-Hei Choi, Chi-Wa Chao, Chi-Seng Lam, Cheng Gong, Chi-Kong Wong, and Man-Chung Wong

FEATURES

Fast dynamic response

Small steady-state error

Low output current ripples

DESCRIPTION

Compared with the conventional active power filter (APF), the LC-coupling hybrid active power filter (LC-HAPF) has a distinct characteristics of low DC-link operating voltage, which can lower the system and operational costs.

Conventional hysteresis PWM controller, adaptive hysteresis PWM controller, proportional-integral (PI) and proportional-resonant (PR) controller have been developed in succession for the LC-HAPF. However, they suffer from different drawbacks, such as varying frequency, large steady-state error, poor disturbance rejection, thus affecting the component design and compensation performance of LC-HAPF

This work proposes a deadbeat current controller for the LC-HAPF. The key concept of this controller is to find out the duty ratio of the switching devices in every fixed switching period based on the LC-HAPF system parameters, sampling period, sensed instantaneous load voltage, compensation current and coupling capacitor voltage signals. Moreover, the mathematical modeling, stability issue and controller's parameter design are also given and discussed.

Comparing to the existing controller of the LC-HAPF, the proposed deadbeat current controller can track with the reference compensation current with low steady-state error and fast dynamic response. Moreover, it can lead LC-HAPF to be operating at a fixed switching frequency with low output current ripples, that reducing the size of the filtering circuit.

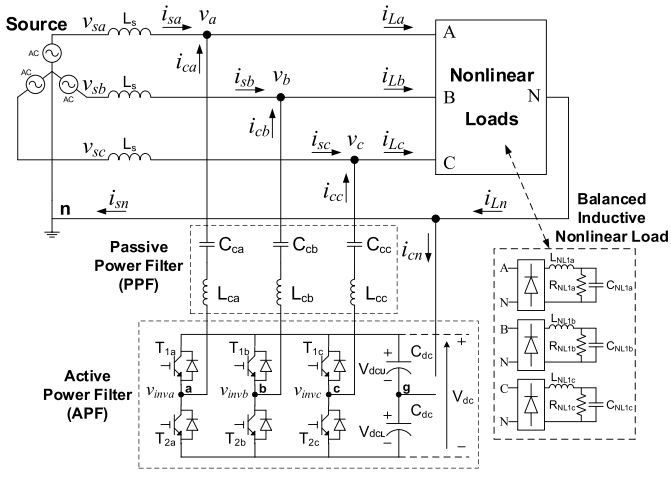


Fig. 1. System configuration of a three-phase four-wire center-split LC-HAPF.

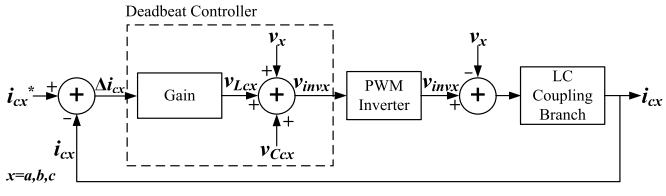


Fig. 2. Control block diagram of deadbeat current controller.

Publication(s)

[1] W.-K. Sou, W.-H. Choi, C.-W. Chao, C.-S. Lam, C. Gong, C.-K. Wong, M.-C. Wong, "A Deadbeat Current Controller of LC-Hybrid Active Power Filter for Power Quality Improvement," IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 8, no. 4, pp. 3891-3905, Dec. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery

Wen-Liang Zeng, Edoardo Bonizzoni, Chi-Wa U, Chi-Seng Lam, Sai-Weng Sin, U-Fat Chio, Franco Maloberti, and Rui P. Martins

FEATURES

Bond-wire inductor

Fast transient recovery

Low power SAR ADC included

Silicon verified in ST 65 nm CMOS

DESCRIPTION

The system block diagram of a successive-approximation-register (SAR) analog-to-digital converter (ADC) assisted DC-DC buck converter is proposed in in Fig. 1, which operates in discontinuous conduction mode (DCM) and achieves fast load transient recovery characteristics. The power inductor of the buck converter uses the bond-wire inductance. During the load transient, the dynamic low-power SAR ADC samples the converter's undershoot/overshoot output voltage and controls the programmable current pump circuit to charge/discharge the output capacitor, thus speeding up and smoothing the load transient response.

The chip fabricated in a 65-nm CMOS technology occupies an area of 1 mm² as shown in Fig. 2. The converter, switching at 100 MHZ, achieves a peak power efficiency of 81% when V_{IN} = 1.2 V, V_{OUT} = 1 V and I_{Load} = 50 mA. When the load current steps from 2 mA to 50 mA,the measured undershoot/overshoot voltage is 101/92 mV, and the recovery time is 175/406 ns.

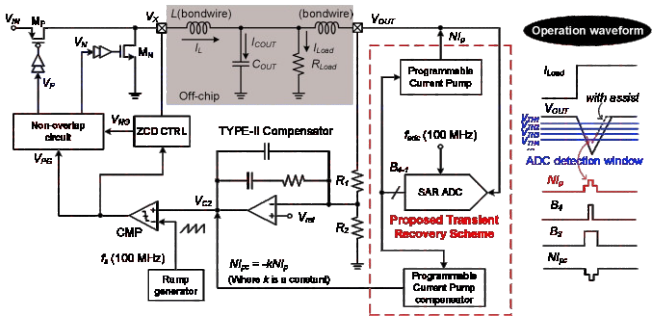


Fig. 1. System block diagram and conceptual waveforms of the proposed buck converter with the SAR assisted transient recovery scheme.

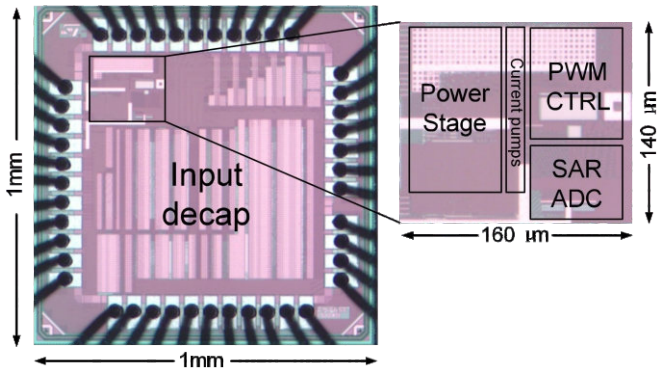


Fig. 2. Chip micrograph.

Publication(s)

[1] W.-L. Zeng, E. Bonizzoni, C.-W. U, C.-S. Lam, S.-W. Sin, U-F. Chio, F. Maloberti, and R. P. Martins, "A SAR-ADC-Assisted DC-DC Buck Converter with Fast Transient Recovery", IEEE Transactions on Circuits and Systems II - Express Briefs, vol. 67, no. 9, pp. 1669 – 1673, Sept. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging

Zhicong Huang, Chi-Seng Lam, Pui-In Mak, Rui P. Martins, Siu-Chung Wong, and Chi K. Tse

FEATURES

Single-stage IPT converter

Constant-power (CP) output

Load impedance matching (High charging efficiency)

Fixed operating frequency

Non-communication-based control

Zero voltage switching

DESCRIPTION

In general, it is challenging for an inductive power transfer (IPT) converter to achieve the required output for constant-power (CP) charging and maintain the maximum efficiency throughout the charging process while permitting fixed operating frequency, soft switching, no extra cascading converter, and no wireless feedback communication. Aimed at filling the gap of wireless CP charging, this work explores a single-stage IPT converter operating as a wireless CP and maximum-efficiency battery charger. By maintaining a constant output power rather than providing a constant output current throughout the dominant stage of battery charging, the IPT converter can make the utmost of its power capability, thus having a faster charging rate.

The proposed single-stage IPT converter adopts series–series compensation and includes a switch-controlled capacitor (SCC) and a semi-active rectifier (SAR) in the secondary side. Manipulating the SCC and the SAR to emulate the optimum impedance of the resonator and the load, we propose a novel operation approach combining the merits of load-independent transfer characteristic and load impedance matching, to achieve a simple solution to CP charging and maximum efficiency throughout the charging process. Since the control scheme is based on fixed operating frequency and secondary-side real-time regulation, no wireless feedback communication is needed for the control, and all power switches realize Zero voltage switching.

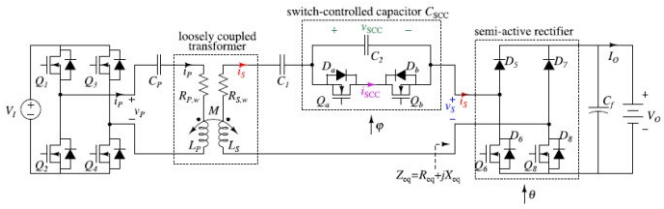


Fig. 1. Schematics of the proposed wireless CP charging system.

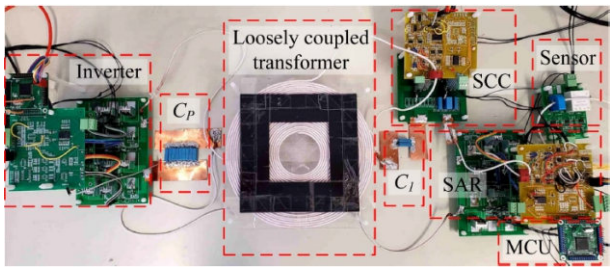


Fig. 2. Experimental Prototype of the proposed CP charging system.

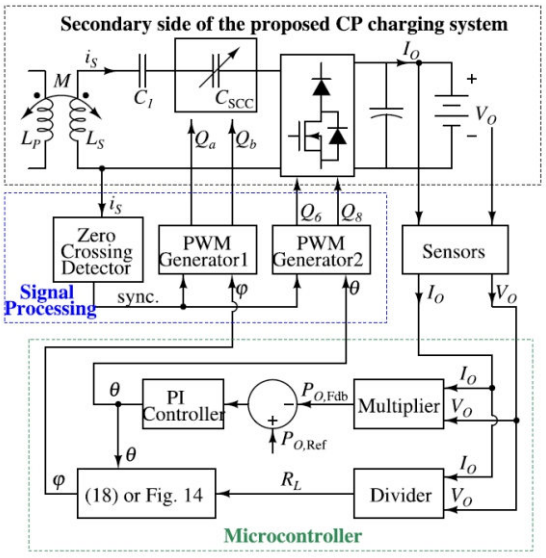


Fig. 3. Secondary load impedance matching control diagram of the proposed CP charging system.

Publication(s)

[1] Z. Huang, C.-S. Lam, P.-I. Mak, R. P. Martins, S.-C. Wong and C. K. Tse, "A Single-Stage Inductive-Power-Transfer Converter for Constant-Power and Maximum-Efficiency Battery Charging," IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 8973-8984, Sept. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Adaptive Thyristor Controlled LC – HAPF for Reactive Power and Current Harmonics Compensation with Switching Loss Reduction

Chi-Seng Lam, Lei Wang, Sut-Ian Ho, and Man-Chung Wong

FEATURES

A simplified minimum V_{dc} calculation for thyristor controlled LC-coupling hybrid active power filter

Reduce a large number of calculation steps

Adaptive DC-link voltage controller for TCLC-HAPF in obtaining low switching loss & noise

DESCRIPTION

An adaptive DC-link voltage controlled thyristor controlled LC-coupling hybrid active power filter (TCLC-HAPF) is proposed for reducing switching loss, switching noise and enhancing the compensating performance. Unfortunately, the TCLC-HAPF has both controllable active TCLC part and active inverter part, thus the conventional minimum DC-link voltage calculation methods for active power filter (APF) and LC-coupling hybridactive power filter (LC-HAPF) cannot be directly applied to the TCLC-HAPF. Moreover, the aforementioned DC-link voltage calculation methods were developed based on the Fast Fourier Transform (FFT), which makes the calculation complex.

This work also presents a simplified minimum DC-link voltage calculation method for TCLC-HAPF reactive power and current harmonics compensation, which can significantly reduce the large amount of the calculation steps by using the FFT method. After that, an adaptive DC-link voltage controller for the TCLC-HAPF is developed to dynamically keep its operating at its minimum DC-link voltage level to reducing its switching loss and switching noise. Representative experimental results are given to verify the proposed simplified DC-link voltage calculation method and the adaptive DC-link voltage control method of TCLC-HAPF.

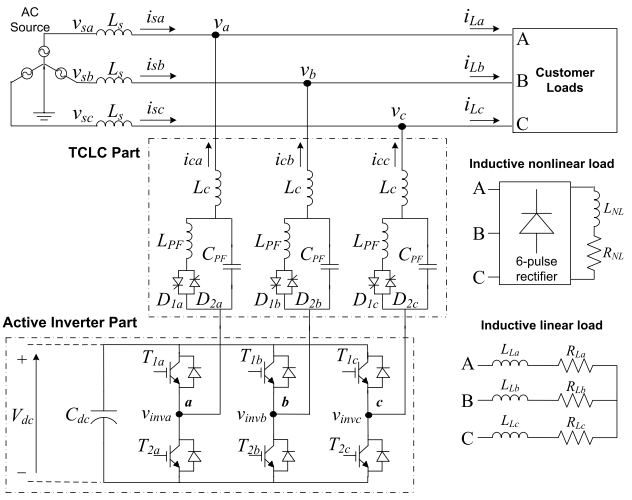


Fig. 1. Circuit configuration of a three-phase three -wire TCLC-HAPF

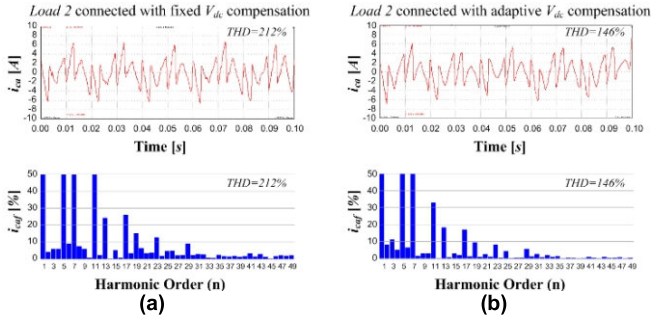


Fig. 2. Experimental i_{ca} and its frequency spectrum with: (a) fixed V_{dc}=60V and (b) adaptive V_{dc} control for Load 2.

Case:	Power Loss [W]	
	Fixed $V_{dc} = 60V$	Adaptive V_{dc}
Load 1	*141W*	*117W ($V_{dc} = 30V$), ↓17%*
Load 2	*147W*	*120W ($V_{dc} = 40V$), ↓18%*

Table 1. Experimental VSI power loss between fixed and adaptive V_{dc} controlled TCLC-HAPF

Publication(s)

[1] C.-S. Lam, L. Wang, S.-I. Ho, M.-C. Wong, "Adaptive Thyristor Controlled LC – Hybrid Active Power Filter for Reactive Power and Current Harmonics Compensation with Switching Loss Reduction," IEEE Transactions on Power Electronics, vol. 32, no. 10, pp. 7577 – 7590, Oct. 2017.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

Analysis, Control and Design of Hybrid Grid-Connected Inverter for Renewable Energy Generation with Power Quality Conditioning

Lei Wang, Chi-Seng Lam, and Man-Chung Wong

FEATURES

A full-bridge three-phase DC/AC inverter in series with a thyristor controlled LC filter

Wide operational range

Low DC-link voltage

DESCRIPTION

A new type DC/AC inverter named: hybrid-coupling grid-connected inverter (HGCI) for Photovoltaic (PV) active power generation with power quality conditioning is proposed, which consists of a full-bridge three-phase DC/AC inverter coupling to the power grid in series with a thyristor controlled LC (TCLC) filter. Compared with the conventional inductive-coupling grid-connected inverter (IGCI) and capacitive-coupling grid-connected inverter (CGCI), the proposed HGCI has distinct characteristics of wide operational range and low DC-link operating voltage. Based on these prominent characteristics, the system cost and operational cost can be reduced. Moreover, it can transfer the active power and compensate reactive power, unbalanced power and harmonic power simultaneously. In this paper, the analysis of the structure, parameter design and control method of the HGCI are proposed and presented. Finally, simulation and experimental results are provided to verify the effectiveness and performance of the proposed HGCI in comparison with the IGCI and CGCI.

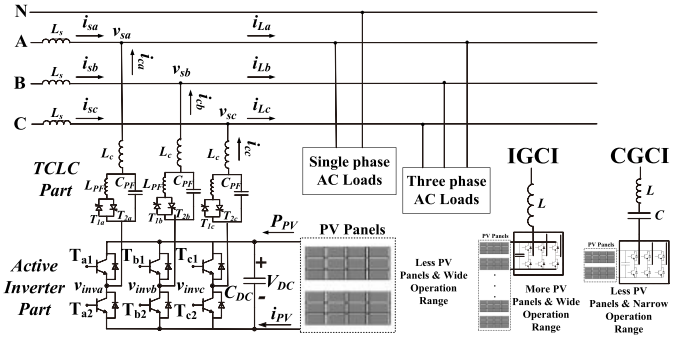
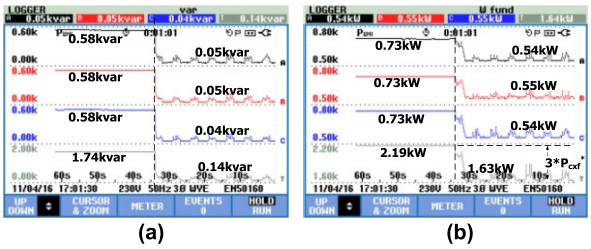


Fig. 1. The structure of the IGCI, CGCI and the proposed HGCI for PV active power injection with power quality conditioning.



(a) (b)

Fig. 3. Dynamic balanced inductive loads compensation by using the HGCI: (a) Q_{sxf} (reactive power compensation) and (b) P_{sxf} (active power injection).

Fig. 2. Experimental setup of the 110V-10A HGCI experimental prototype.

Publication(s)

[1] L. Wang, C.-S. Lam, M.-C. Wong, "Analysis, control, and design of a hybrid grid-connected inverter for renewable energy generation with power quality conditioning", IEEE Transactions on Power Electronics, vol. 33, no. 8, pp. 6755 – 6768, Aug. 2018

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter

Zhicong Huang, Zhijian Fang, Chi-Seng Lam, Pui-In Mak, and Rui P. Martins

FEATURES

Load-independent-voltage outputs with ZPA input

Efficiency enhancement

Optimization of the compensation capacitance cost

DESCRIPTION

Load-independent output with zero-phase angle (ZPA) input is desirable in wireless inductive power transfer (IPT) converters for effective power delivery, but it usually greatly relies on the parameters of the loosely coupled transformer, normally fixed or constrained by space. However, customizable outputs cannot be readily achieved unless a new transformer is redesigned. Thus, in this work, a cost-effective compensation design is elaborated to achieve customizable LIV outputs with ZPA input and optimized power efficiency for the S/SP IPT converter. Parameters of three compensation capacitors of a S/SP IPT converter were indicated by a single factor μ, which simplifies the analysis of the relationships among compensation parameters, customizable LIV outputs with ZPA input, power efficiency, and overall compensation capacitance cost. Critical values of μ ensuring load impedance matching for optimized efficiency, achieving minimum overall compensation capacitance and limiting overall compensation capacitance for effective cost were respectively derived for guiding the design.

Compared with a conventional design, the proposed design provides custom ranges of LIV outputs in both a weak and a relatively strong coupling condition, with over 5.9% and 5% efficiency improvement, respectively. The overall compensation capacitance can also be reduced by up to 37% and 21.5%, respectively.

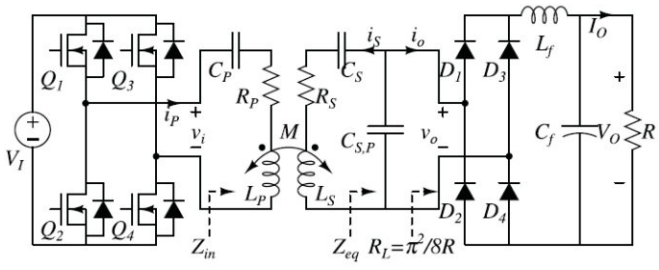


Fig. 1. (a) Schematics and (b) equivalent circuit model of the S/SP IPT converter.

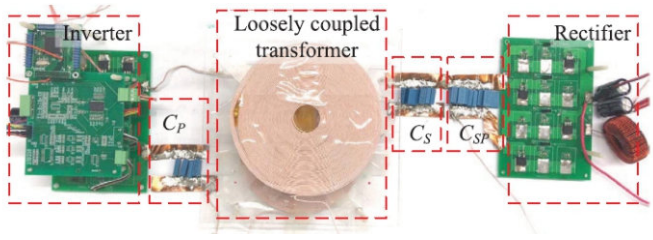


Fig. 2. Experimental Prototype of the S/SP IPT converter.

Publication(s)

[1] Z. Huang, Z. Fang, C. -S. Lam, P. -I. Mak and R. P. Martins, "Cost-Effective Compensation Design for Output Customization and Efficiency Optimization in Series/Series-Parallel Inductive Power Transfer Converter," IEEE Transactions on Industrial Electronics, vol. 67, no. 12, pp. 10356-10365, Dec. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

Effects of Parasitic Resistances on Magnetically Coupled Impedance-Source Networks

Xiangfei Kong, Chi-Kong Wong, and Chi-Seng Lam

FEATURES

Magnetically coupled impedance-source networks

Generalized equivalent circuit model

Voltage gain under parasitic resistances

DESCRIPTION

Magnetically coupled impedance-source networks can achieve a higher voltage gain with smaller shoot-through duty ratio in comparison with the conventional impedance-source networks without coupled inductors. However, the practical voltage gain is seriously affected by the parasitic resistances in passive components and power devices, which is necessary to be investigated. This work derives and analyzes the effects of parasitic resistances on the voltage gain of magnetically coupled impedance-source networks under three different scenarios: 1) different resistance ratio between parasitic resistances and output equivalent resistance, 2) different shoot-through duty ratio and 3) different winding ratio.

First of all, a generalized equivalent circuit model considering parasitic resistances for the three typical magnetically coupled impedance-source networks – Trans-Z-source, Γ-source and Y-source networks are proposed. Based on it, the effects of parasitic resistances on the voltage gain is mathematically derived and discussed under the aforementioned three different scenarios. And the maximum voltage gain under the consideration of the three resistance ratios simultaneously is also derived. Finally, representative simulation and experimental results are provided to verify the proposed generalized equivalent circuit models, the corresponding mathematical derivations, and the effects of the parasitic resistances on the magnetically coupled impedance-source networks.

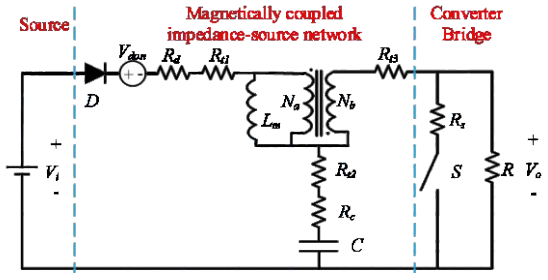


Fig. 1. Equivalent circuit model of magnetically coupled impedance-source converter under parasitic resistances condition

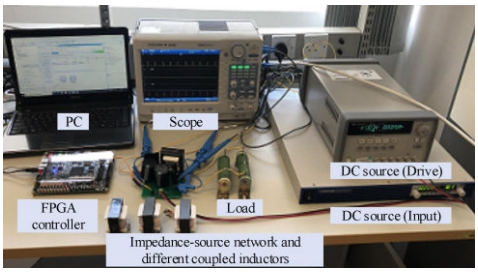


Fig. 2. Experimental prototype of the magnetically coupled impedance-source converter

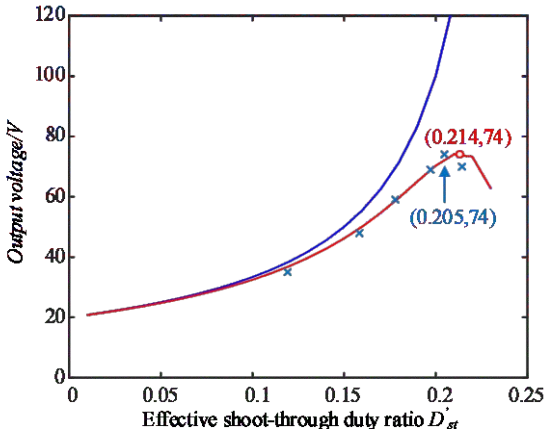


Fig. 3. Comparison of idea lossless, theoretical and experimental results of Trans-Z-source network with N_1:N_2=36:12

Publication(s)

[1] X. Kong, C.-K. Wong, Chi-Seng Lam, "Effects of Parasitic Resistances on Magnetically Coupled Impedance-Source Networks," IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9171 – 9183, Sept. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau

A Hybrid Boost Converter With Cross-Connected Flying Capacitors

Mo Huang, Yan Lu, Tingxu Hu, and Rui P. Martins

FEATURES

Hybrid DC-DC boost converter

Good efficiency for > 4 conversion ratio

Flying capacitors soft charging

Halved output voltage ripple

Cascade bootstrap

Silicon verified in AMS 0.35-µm CMOS

DESCRIPTION

It is a hybrid DC-DC boost converter suitable for high conversion ratio (CR) applications. The performance and area are advanced in fivefold: 1) the topology halves the stress of most power switches, reducing the dynamic power loss and area; 2) the high CR is achieved with doubled pulse width of the gate control signals, allowing a higher switching frequency; 3) the inductor current ripple is reduced from the halved switching node voltage swing and increased switching frequency, then a high DCR (or small-volume) inductor can be used; 4) the flying capacitors (Cfly) are soft charged, allowing to use a small Cfly value. This significantly reduces the Cfly volume under a high voltage application. 5) the cascade bootstrap scheme reuses the bootstrap capacitor between two working phases.

Fabricated in 0.35-µm CMOS, the converter measures 93.5% power conversion efficiency (PCE) at CR = 4.5. The Cfly value is reduced to 0.47µF from soft charging. And a 3010-package inductor with 166-mΩ DCR is used. The cascade bootstrap reduces halves the large bootstrap capacitor. The active area is 0.86 mm^2.

Benchmarking with the prior art, this work succeeds in enhancing the PCE under a high CR. Additionally, it significantly reduces the volume of the inductors and Cflys. Moreover, it doubles the pulse width of the gate control signals, suitable for a high-CR application. Finally, it reduces the silicon area.

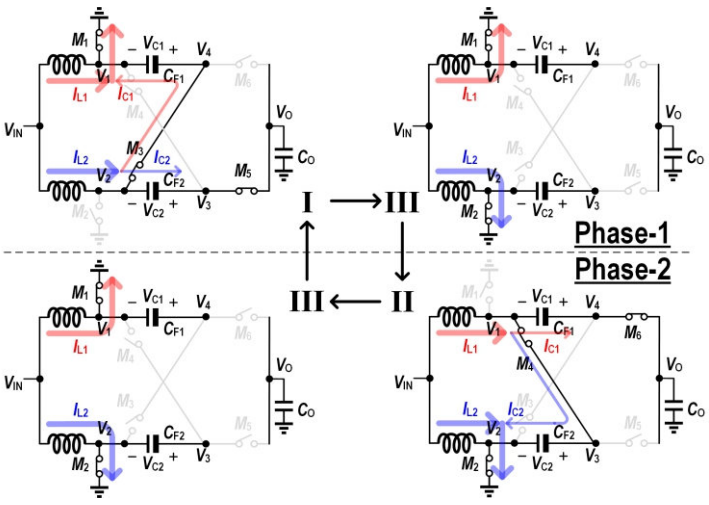


Fig. 1. Proposed convertor working principle.

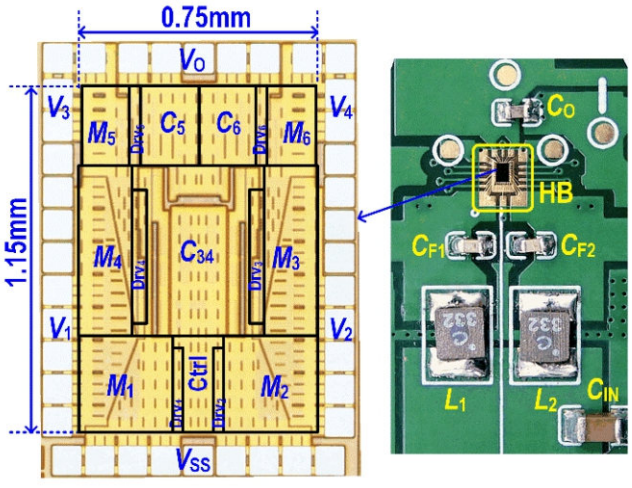


Fig. 2. Chip and PCB photos.

Publication(s)

[1] M. Huang, Y. Lu, T. Hu, and R. P. Martins, “A Hybrid Boost Converter With Cross-Connected Flying Capacitors,” IEEE Journal of Solid-State Circuits, vol. 56, no. 7, pp. 2102–2112, Jul. 2021.

[2] M. Huang, Y. Lu, and R. P. Martins, “A 2-Phase Soft-Charging Hybrid Boost Converter with Doubled-Switching Pulse Width and Shared Bootstrap Capacitor Achieving 93.5% Efficiency at a Conversion Ratio of 4.5,” IEEE International Solid -State Circuits Conference (ISSCC), Digest of Technical Papers, pp. 198–200, Feb. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Natural Science Foundation of China

An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction

Mo Huang, Yan Lu, and Rui P. Martins

FEATURES

Hybrid Low dropout regulator

Analog-proportional digital-integral control

Improved PSR up to 1MHz

Reduced output voltage ripple

Silicon verified in TSMC 65-nm CMOS

DESCRIPTION

It is a hybrid low dropout regulator (LDO) that uses analog-proportional digital-integral control. The slow, discontinuous digital-integral control provides a high DC loop gain under a low supply voltage (Vin). The analog proportional control achieves better performances in threefold: 1) it allows a fast, continuous transient response without increasing the power consumption significantly; 2) it compensates the limit cycle oscillation (LCO) from the discontinuous sampling; 3) it is the only solution to suppress the continuous power supply noise and thus improves the power supply rejection (PSR). The flip voltage follower (FVF) analog part is used, suitable for a low-Vin operation. A replica analog loop is added to further improve the PSR by 6dB. The replica loop also ensures the proportion of the output current shared by the digital control, improving the output voltage accuracy.

Fabricated in 65-nm CMOS, the LDO measures a 0.37ps FoM of speed. The 1-MHz PSR is −22dB under 0.6Vin and 0.1Vdropout. The output LCO is reduced to 3mV at a light load and almost unobservable at a heavy load. The active area is 0.04 mm².

Benchmarking with the prior art, this work succeeds in achieving a comparable high-frequency PSR under a lower supply Vin and Vdropout. Additionally, it responds fast without significantly increasing the power consumption. Finally, it reduces the silicon area.

(a)

(b)

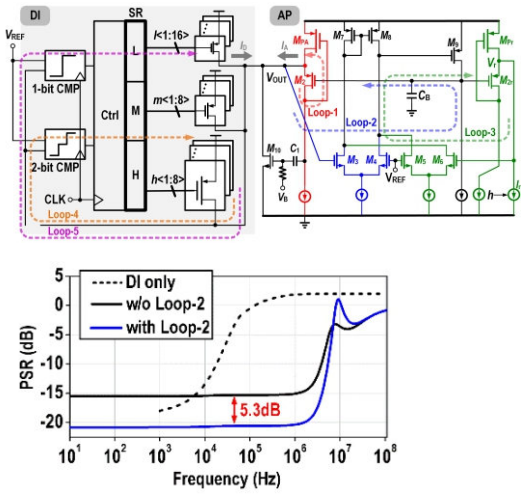


Fig. 1. (a) Schematic of the proposed LDO, and (b) PSR improvement from the replica loop.

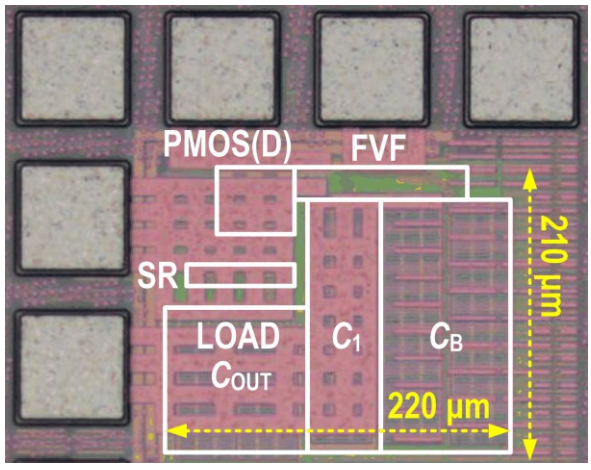


Fig. 2. Chip microphotograph.

Publication(s)

[1] M. Huang, Y. Lu, and R. P. Martins, "An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction," IEEE Journal of Solid-State Circuits, vol. 55, no. 6, pp. 1637–1650, Jun. 2020.

[2] M. Huang and Y. Lu, "An Analog-Proportional Digital-Integral Multi-Loop Digital LDO with Fast Response, Improved PSR and Zero Minimum Load Current," in 2019 IEEE Custom Integrated Circuits Conference (CICC), Apr. 2019.

Sponsorship

Natural Science Foundation of China, Research Committee of University of Macau

An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery

U-Fat Chio, Kuo-Chih Wen, Sai-Weng Sin, Chi-Seng Lam, Yan Lu, Franco Maloberti and R.P. Martins

FEATURES

VCO-based SC 15-phase DC-DC converter

Two embedded transient-enhancement techniques (SFM & MCW)

15-phase interleaved converter

Fast transient response time/ load recovery

Silicon verified in 65 nm CMOS

DESCRIPTION

It presents a fully integrated VCO-based switched-capacitor (SC) 15-phase DC-DC converter in 65 nm CMOS. We propose two transient-enhancement techniques: Segmented Frequency Modulation (SFM) and Multiphase Co-Work control (MCW) to reduce the latency of the VCO-based control loop and shorten the SC DC-DC converter's transient response time.

The SFM can improve the heavy-to-light load transient by dynamically increasing the charge pump discharge current by 9 times, while the MCW can enhance the light-to-heavy load recovery by synchronously combining three interleaved flying capacitors together during the transient state. We designed the 15-phase interleaved converter to support an output voltage of 1 V from a 2.4 V input supply, delivering up to 138 mA of load current, which takes only 25/29 ns for output voltage recovering to the steady state from heavy-to-light/light-to-heavy load transients, respectively.

A prototype was then implemented in 65 nm CMOS. It obtains a peak efficiency of 82.8 % and keeps the efficiency above 80 % from 31 mA to the maximum load current. The SC DC-DC converter chip occupies 0.61 mm², and its output power density is 240 mW/mm². From light-to-heavy and heavy-to-light load transients, the converter can also reach a fast recovery speed of 5.1 mA/ns and 4.38 mA/ns, respectively, reflecting a state-of-the-art transient recovery performance.

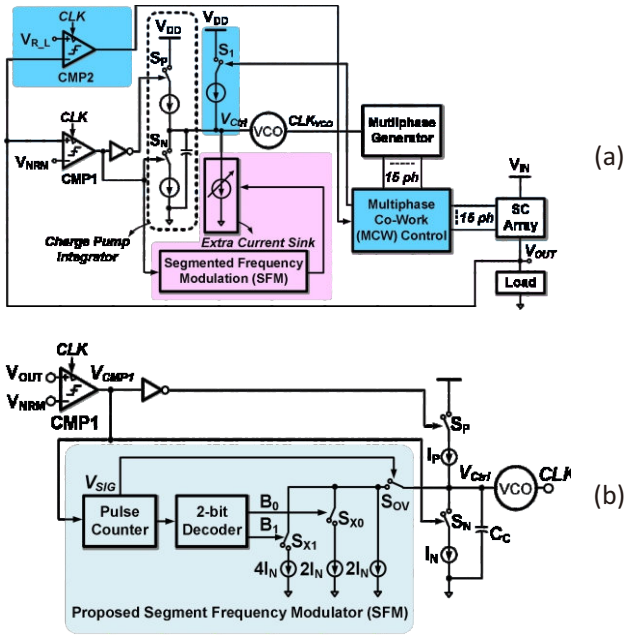


Fig. 1. Block diagram of the proposed Incremental ADC at (a) Linear-Phase and (b) Exponential-Phase.

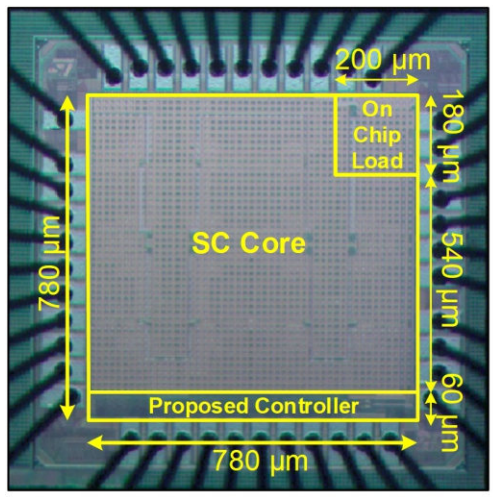


Fig. 2. Chip micrograph.

Publication(s)

[1] U.-F. Chio, K.-C. Wen, S.-W. Sin, C.-S. Lam, Y. Lu, F. Maloberti, and R. P. Martins, "An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery," 2018 IEEE Asian Solid-State Circuits Conference (A-SSCC), 2018, pp. 31-32.

[2] U.-F. Chio, K.-C. Wen, S.-W. Sin, C.-S. Lam, Y. Lu, F. Maloberti, and R. P. Martins, "An Integrated DC–DC Converter With Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery," in IEEE Journal of Solid-State Circuits, vol. 54, no. 10, pp. 2637-2648, Oct. 2019 (Invited Special Issue of A-SSCC).

Sponsorship

AMSV Research Report 2017–21Category Here (Please select in the form) This work was supported by the Research Committee of the University of Macau and Macao Science and Technology Development Fund SKL-AMSV-2017-2019 (DP), SKL/AMS-VLSI/SSW/FST and SKL/AMS-VLSI/WMC/FST under Grant 120/2016/A3.

A Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays

Fangyu Mao, Yan Lu, Edoardo Bonizzoni, Filippo Boera, Mo Huang, Franco Maloberti, and Rui P Martins

FEATURES

For AMOLED display driver

Single-inductor bipolar-output DC-DC

Hybrid power conversion

Floating negative output for small positive ripple

3.5W maximum output power

Silicon verified in 0.35µm CMOS

DESCRIPTION

This work is a hybrid single-inductor bipolar-output (SIBO) DC-DC converter for active-matrix organic light-emitting diode (AMOLED) displays, which are relatively more sensitive to the supply noise on the positive supply. Firstly, to improve the display quality we adopt a floating negative output configuration to migrate all the switching ripples into the negative output, achieving a near-zero voltage ripple on the positive output. Secondly, we design low-power shunt regulators, which only deal with a small portion of the output ripple, to regulate the positive output voltage further, improving the load transient response. Besides, the hybrid topology and the proposed cross-coupled bootstrap-based level-shifter, with a dual-PMOS inverter buffer, only uses standard CMOS devices without deep-N-well, reducing the chip area and cost.

The proposed converter, implemented in 0.35-µm CMOS with 5-V devices, operates at 1 MHz, leading to a measured positive output voltage ripple lower than 1 mV (all conditions). It achieves a measured 3-mV undershoot voltage and, an unnoticeable overshoot voltage on the positive output, when the output current varies between 30 mA and 350 mA. The measured peak power efficiency is 89.3% at 1.1-W output power. The maximum output power is 3.5W.

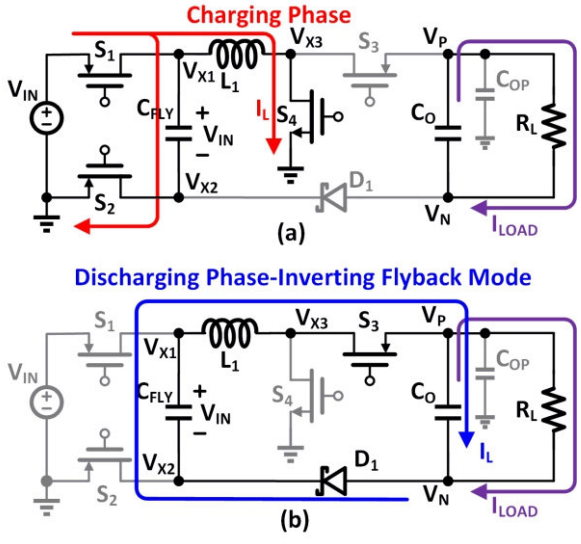


Fig. 1. (a) The charging and (b) the discharging phase of the proposed SIBO converter.

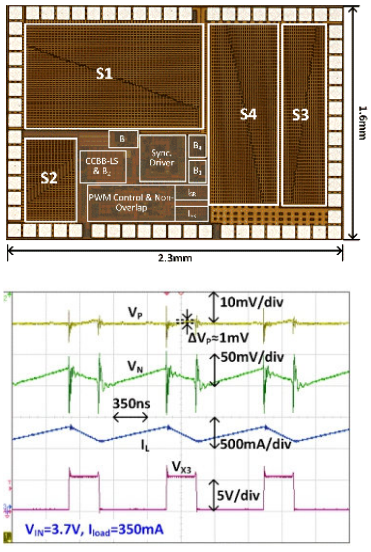


Fig. 2. Chip micrograph, and measured voltage and current waveforms.

Publication(s)

[1] F. Mao et al., "A Hybrid Single-Inductor Bipolar-Output DC-DC Converter With Floating Negative Output for AMOLED Displays," IEEE Journal of Solid-State Circuits, early access online.

[2] F. Mao et al., "A Power-Efficient Hybrid Single-Inductor Bipolar-Output DC-DC Converter with Floating Negative Output for AMOLED Displays," in IEEE Custom Integrated Circuits Conference (CICC), Mar. 2020.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation

Jie Lin, Yan Lu, Chenchang Zhan, and R. P. Martins

FEATURES

For fully wireless devices
Single-stage regulating rectifier
Dual output without additional power MOSFET
Fast response with hysteretic current-wave modulation
6.78 MHz resonant frequency
Silicon verified in 0.18µm CMOS

DESCRIPTION

This work is a 6.78-MHz single-stage dual-output regulating rectifier for miniaturizing the true-wireless devices. The proposed rectifier topology realizes AC-DC power conversion and dual-output voltage regulation simultaneously in one single stage, using only four on-chip power transistors, thereby reducing chip area and off-chip components, and improving the system power conversion efficiency. We integrate high voltage (HV) and low voltage (LV) transistors in the proposed dual-output rectifier for HV and LV output voltages, respectively. The proposed two independent three-level current-wave modulation (CWM) controllers realize voltage conversion and regulation for each output independently, with instant transient response and no cross-regulation problem.

The proposed dual-output regulating rectifier, fabricated in 0.18-µm CMOS using 1.8/3.3-V devices, can deliver a total maximum power of 1.02 W at the dual-output voltages of 1.8 V and 3.3 V. The circuit achieves a measured peak efficiency of 91.9 % with an instant load-transient response for a load current step between 20 mA and 200 mA. The cross-regulation between the dual-output voltages is unnoticeable.

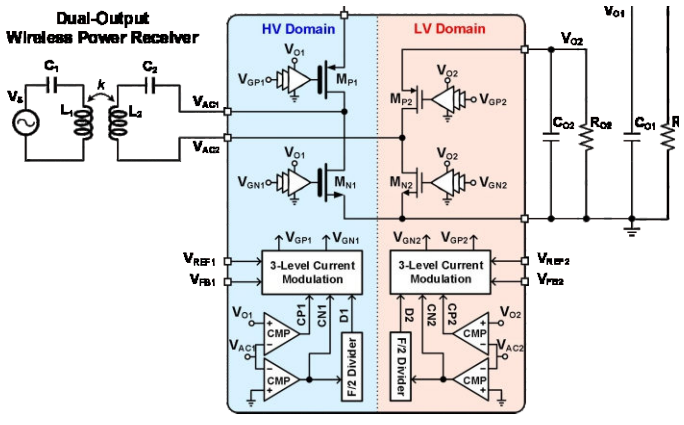


Fig. 1. A wireless power receiver with the proposed dual-output rectifier.

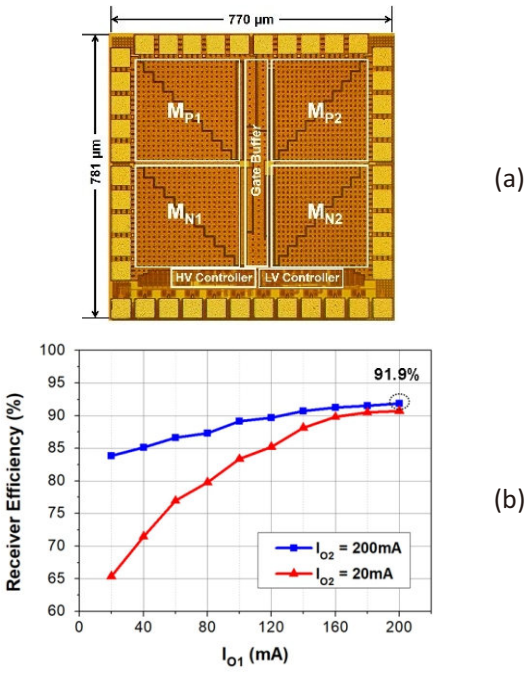


Fig. 2. (a) Chip micrograph, and (b) measured efficiency.

Publication(s)

[1] J. Lin, Y. Lu, C. Zhan, and R. P. Martins, "A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation," IEEE Journal of Solid-State Circuits, early access online.

[2] J. Lin, C. Zhan, and Y. Lu, "A 6.78-MHz Single-Stage Wireless Power Receiver with Ultra-Fast Transient Response Using Hysteretic Control and Multi-Level Current-Wave Modulation," IEEE Transactions on Power Electronics, vol. 36, no. 9, pp. 9918–9926, Sep. 2021.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau, Shenzhen STI Fund.

A VHF Wide-Input Range CMOS Passive Rectifier with Active Bias Tuning

Xiaofei Li, Fangyu Mao, Yan Lu, and Rui P. Martins

FEATURES

RF wireless power transfer

Passive rectifier with active bias tuning

Average maximum efficiency of 64.4%

Silicon verified in 65nm CMOS

DESCRIPTION

Tiny implantable medical devices in mm-size demand advanced wireless power solutions that operate at hundreds of MHz, and mainly use passive rectifiers for AC-DC power conversion. A conventional cross-connected (CC) rectifier can operate with high frequency and low input voltage, but only achieves good efficiencies in a very narrow input power range, due to the shoot-through and reverse currents. This work presents a CMOS passive rectifier with active bias tuning (ABT), allowing a widely extended input range with high power conversion efficiency. In addition, we compensate the process, voltage, and temperature variations with the ABT scheme that leads to a robust design for very high frequency (VHF) operation. Meanwhile, we propose a peak V_{OUT} searching scheme to indicate the charging or discharging directions for the ABT. We obtain a bias voltage balancing among stacked rectifier stages with a switched-capacitor network.

The proposed rectifier is fabricated in a 65-nm CMOS process. Measurement results of three chips show that the proposed rectifier improves the PCE over a wide input range, with an average maximum PCE of 64.4%.

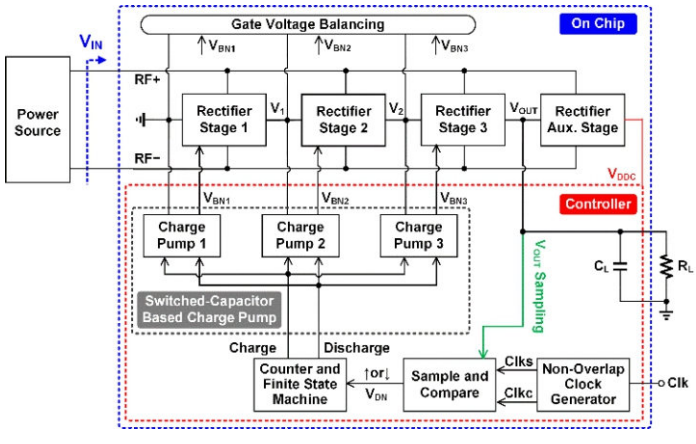


Fig. 1. System overview of the proposed rectifier with active bias tuning.

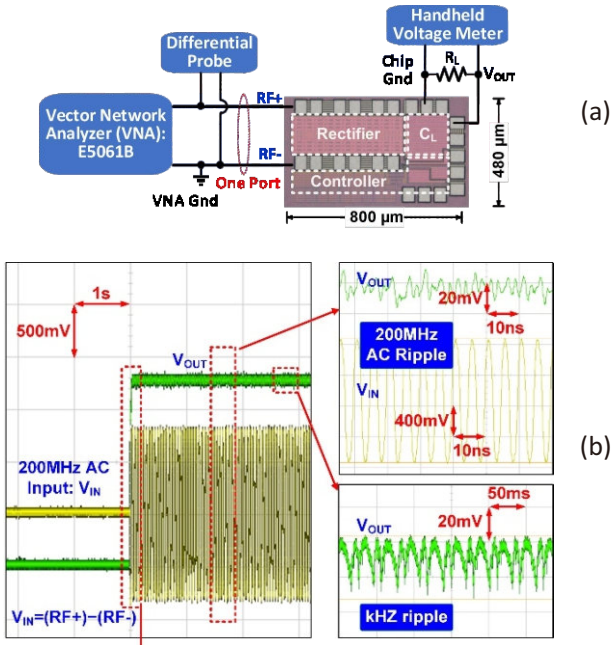


Fig. 2. Chip micrograph, and measured input and output voltage waveforms.

Publication(s)

[1] X. Li, F. Mao, Y. Lu, and R. P. Martins, "A VHF Wide-Input Range CMOS Passive Rectifier With Active Bias Tuning," IEEE Journal of Solid-State Circuits, vol. 55, no. 10, pp. 2629–2638, Oct. 2020.

[2] X. Li, F. Mao, P. Yeon, Y. Lu, M. Ghovanloo, and R. P. Martins, "A 200-MHz Wide Input Range CMOS Passive Rectifier with Active Bias Tunning," in IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2019, pp. 245–246.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

An NMOS Digital LDO with NAND-Based Analog-Assisted Loop in 28-nm CMOS

Xiaofei Ma, Yan Lu*, Qiang Li, Wing-Hung Ki, and Rui P. Martins

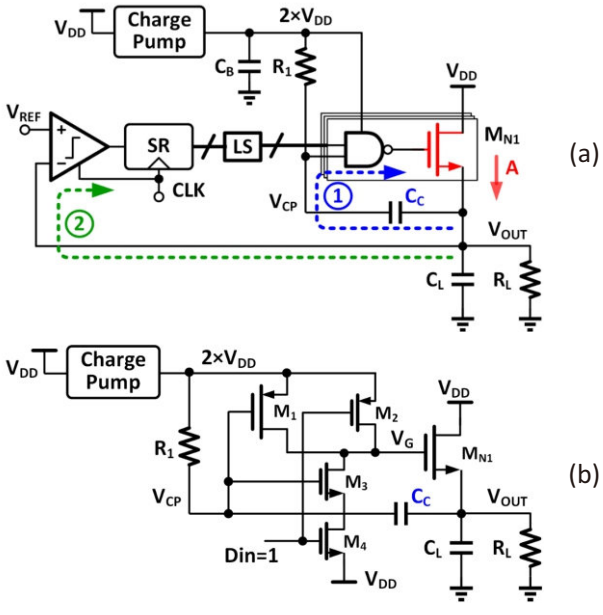
FEATURES

Analog-assisted digital control
NMOS low-dropout regulator
Output-capacitor free
<1μA quiescent current
Silicon verified in 28nm CMOS

DESCRIPTION

This work is an NMOS digital low-dropout regulator (LDO) with fast transient response and ultra-low quiescent current, to provide a tunable power supply for near-threshold voltage computing circuits in internet-of-things (IoT) devices. An LDO with an NMOS power transistor can enjoy the intrinsic fast transient response of the source-follower-like power stage, contributing to the proportional (P) part of the control loop. A shift-register-based digital control serves as an excellent candidate for the integral (I) part of the control loop. In addition, we propose a NAND-gate-based high-pass analog path (NAP) as the derivative (D) part of the loop, making the whole control scheme a complete PID control, therefore, achieving a fast transient response.

We fabricated two versions of the prototype chip, one with a 30-pF on-chip load capacitor and a fast-transient on-chip load, and the other with no load capacitor, in 28-nm CMOS. The proposed NMOS digital LDO with NAP can handle the load transient of 160 mA/ns with 810-nA quiescent current, achieving 117-mV voltage undershoot. With the proposed techniques, we can achieve nearly two orders of better FoM when comparing it to the state-of-the-art works.



(a)

(b)

Fig. 1. (a) The proposed NMOS DLDO with NAND-based high-pass analog path, and (b) the Schematic of NAP.

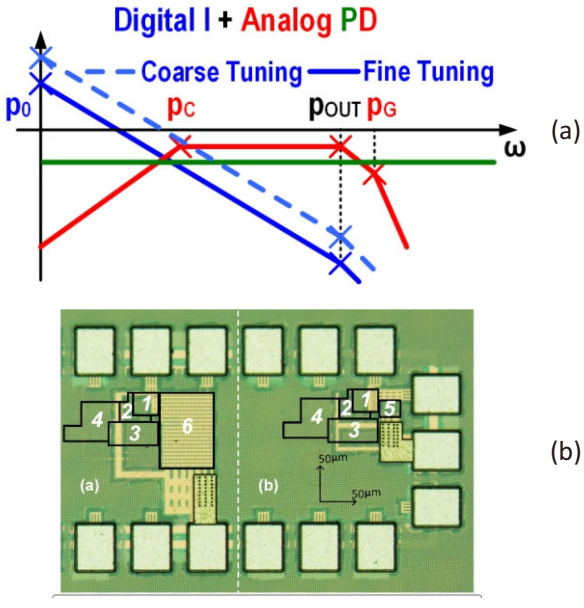


Fig. 2. The frequency responses of the loops, and the die photo of the two proposed design.

Publication(s)

[1] X. Ma, Y. Lu, Q. Li, W.-H. Ki, and R. P. Martins, "An NMOS Digital LDO With NAND-Based Analog-Assisted Loop in 28-nm CMOS," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 67, no. 11, pp. 4041–4052, Nov. 2020.

[2] X. Ma, Y. Lu, R. P. Martins, and Q. Li, "A 0.4V 430nA quiescent current NMOS digital LDO with NAND-based analog-assisted loop in 28nm CMOS," in IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2018, pp. 306–308.

Sponsorship

Macau Science and Technology Development Fund (FDCT), Research Committee of University of Macau.

LIST OF PATENTS

1. Man-Chung Wong, Chi-Seng Lam, Lei Wang, “A Hybrid STATCOM with wide compensation range and low dc-link voltage”, Application No. 15/425,270, US Utility Patent, February 2017

2. Lei Wang, Man-Chung Wong, Chi-Seng Lam, “Design of a thyristor controlled LC compensator”, Application No. 15/614,672, US Utility Patent, June 2017

3. Pui-In Mak, Zhicheng Lin, R. P. Martins, “Radio-Frequency-to-baseband function-reuse receiver with shared amplifiers for common-mode and differential-mode amplification”, US Patent, No. 9,673,781, June 2017.

4. Pui-In Mak, Zhicheng Lin, R. P. Martins, “Gain-boosted N-path passive-mixer-first receiver with a single mixing step”, US Patent, No. 9,680,448, June 2017.

5. Man-Chung Wong, Chi-Seng Lam, Yan-Zheng Yang, Wai-Hei Choi, Ning-Yi Dai, Yajie Wu, Chi-Kong Wong, Sai-Weng Sin, U-Fat Chio, Seng-Pan U, R. P. Martins, “Mixed signal controller”, US Patent, No. 9,692,232, June 2017

6. Tianlan Chen, Cheng Dong, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, R. P. Martins, “Electronic module for real-time droplet-position sensing and driving in digital microfluidic system”, US Patent, No. 9,751,083, September 2017.

7. Man-Chung Wong, Chi-Seng Lam, Lei Wang, “A hybrid grid connected power generation inverter system with power quality compensation”, Application No. CN201710980413.4, Chinese Patent for Invention, October 2017

8. Tianlan Chen, Cheng Dong, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, R. P. Martins, “Electrode -voltage waveform for droplet-velocity and chip-lifetime improvements of digital microfluidic systems”, US Patent, No. 9,808,800, November 2017.

9. Mo Huang, Yan Lu, Sai-Wang Sin, Seng-Pan U, R. P. Martins, “Limit cycle oscillation reduction for digital low dropout regulators”, US Patent, No. 9,946,281, April 2018.

10. Tianlan Chen, Cheng Dong, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, R. P. Martins, “一種檢測和分析 DNA 的 方 法 ” (A method for testing and analyzing DNA), China Patent, No. CN107937485A, WO2019128081A1 (PCT), April 2018.

11. Tianlan Chen, Cheng Dong, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, R. P. Martins,“一種檢測和分析 DNA 的 方 法 ” International Patent, PCT/CN2018/088762, May 2018.

12. Lei Wang, Man-Chung Wong, Chi-Seng Lam, “Design of a Thyristor Controlled LC Compensator,” US Utility Patent, No. 9,960,599, May 2018.

13. Man-Chung Wong, Chi-Seng Lam, Lei Wang, “A Hybrid STATCOM with Wide Compensation Range and Low DC-Link Voltage” US Utility patent, No. 10,003,195, June 2018.

14. Yanwei Jia, Haoran Li, Ren Shen, Cheng Dong, Tianlan Chen, Jie Gao, Pui-In Mak , R. P. Martins, “A Method for On-Chip Precise Sample Delivery in a Microfluidic System”, International Patent, PCT /UMPT161-2018, July 2018.

15. Tianlan Chen, Cheng Dong, Jie Gao, Yanwei Jia, Pui-In Mak, Mang-I Vai, R. P. Martins, “Cooperative -electrode driving technique for droplet-velocity improvement of digital microfluidic systems”, US Patent, No. 10,016,759, July 2018.

16. Yan Lu, Mo Huang, Seng-Pan U, R. P. Martins, “Reconfigurable bidirectional wireless charging transceiver”, US Patent, No. 10,256,661, April 2019.

17. Ada Hang-Heng Wong, Chuxia Deng, Yanwei Jia, Haoran LI, Pui-In Mak, R. P. Martins, Yan Liu, Chi-Man Vong, Hang-Cheong Wong, PAK-Kin Wong, Haitao Wang, Heng Sun, “Droplet Microfluidics for Drug Screening”, US Patent, No. 20190291112, September 2019.

18. Ka-Meng Lei, Pui-In Mak, Man-Kay Law, R. P. Martins, “Palm-size μ NMR relaxometer using a digital microfluidic (DMF) device and a semiconductor transceiver for chemical/biological diagnosis”, US Patent, No. 10,436,726, October 2019.

19. Yanwei Jia, Liang Wan, Cheng Dong, Haoran Li, Tianlan Chen, Pui-In Mak, R. P. Martins, “Digital Microfluidics for Polymerase Chain Reaction”, US Patent, No. 20190358636, November 2019.

20. Yanwei Jia, Ren Shen, Pui-In Mak, R.P.Martins, “增強核酸擴增反應的增強劑、試劑盒和進行核酸擴 增反應的方法” (Enhancer for enhancing nucleic acid amplification reaction, kit and method for performing nucleic acid amplification reaction), China Patent, No. CN110628877A, December 2019.

21. Yanwei Jia, Haoran Li, Ren Shen, Cheng Dong, Tianlan Chen, Jie Gao, Pui-In Mak , R. P. Martins, “Apparatus and Method for On-Chip Microfluids Dispensing”, WO Patent, WO2020024119A1, February 2020.

22. Chi-Seng Lam, Zhicong Huang, Pui-In Mak, R.P.Martins, “無線充電電路和系統” (Wireless charging circuit and system), China Patent, No. CN110957796A, April 2020.

23. Biao Wang, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, R. P. Martins, “Single-Loop Linear-Exponential Multi-Bit Incremental Analog-to-Digital Converter”, US Patent, No. 10,644,718 B1, May 2020

24. Jie Lin, Chenchang Zhan, Yan Lu, R. P. Martins, “多路輸出有源整流器結構和無線充電電路” (Multipath output active rectifier structure and wireless charging circuit), China Patent, No. CN111464051A, July 2020.

25. Zhicong Huang, Chi-Seng Lam, Pui-In Mak, R. P. Martins, “Wireless Charging Circuit and System”, Chinese Patent for Invention, No. 201911279433.4, July 2020

26. Law Man Kay, Zhiyuan Chen, Mak Pui In, R. P. Martins, “Flipping-capacitor rectifier circuit”, US Patent, No. 10,756,643, August 2020.

27. Jie Lin, Chenchang Zhan, Yan Lu, R. P. Martins, “雙路輸出有源整流器結構和無線充電電路” (Dual-output active rectifier structure and wireless charging circuit), China Patent, No. CN111490690A, August 2020.

28. Yanwei Jia, Haoran Li, Ren Shen, Cheng Dong, Tianlan Chen, Jie Gao, Pui-In Mak , R. P. Martins, “Apparatus and Method for On-Chip Microfluids Dispensing”, US Patent, No. 20200254457, August 2020.

29. Yanwei Jia, Ren Shen, Pui-In Mak, R. P. Martins, “Enhancing Agent and Kit for Enhancing Nucleic Acid Amplification Reaction and Method for Performing Nucleic Acid Amplification Reaction”, US Patent, No. 20200362400, November 2020.

30. Man-Chung Wong, Chi-Seng Lam, Lei Wang, “Hybrid grid-connected power generation inverter system equipped with power quality compensation”, China Patent, No.CN107749639B, December 2020

Digifluidic Biotech Ltd. http://digifluidic.com

Digifluidic Biotech Ltd. is a young and dynamic biotechnology company founded in 2018.

With digital microfluidics as the core technology and automatic nucleic acid analysis system as the main product, Digifluidic is committed to developing precise automatic in vitro diagnostic equipment, whose application fields include medical disease diagnosis, animal and plant disease detection, health index detection, import and export inspection and quarantine, food safety detection, etc., which shows infinite possibilities in the future.

The nucleic acid detection equipment developed by Digifluidic at this stage has the characteristics of small size, easy to carry, simple operation and low cost. It solves the problems that traditional nucleic acid detection requires complex personnel operation and special detection sites. In the future, Digifluidic plans to cooperate with government agencies and scientific research institutions in different fields to develop various detection applications with different detection methods. In the medical field, Digifluidic aims to improve patient care, reduce costs and improve laboratory efficiency; in the non-medical field, Digifluidic aims to develop a variety of applications, improve people's quality of life and efficiency, and provide greater driving force for the future development of precision, automation and miniaturization of detection equipment.

OUR TEAM

SKL-AMSV Leadership Team

Rui Paulo da Silva Martins, Director
Pui-In Mak, Deputy Director & Wireless and Multidisciplinary Innovation Center (WMIC) Coordinator
Sai-Weng Sin, Associate Director (Academic) & Data and Power Conversion Innovation Center (DPIC) Coordinator

SKL-AMSV Faculty

Man-Kay Law, Associate Professor & Laboratory Infrastructure Coordinator
Yan Zhu, Associate Professor & Industrial Collaboration Coordinator
Yan Lu, Associate Professor & Microelectronics Center/ZUMRI Coordinator
Mang-I Vai, Biomedical Research Line Co-Coordinator
Sio-Hang Pun, Associate Professor
Chi-Seng Lam, Associate Professor
Jun Yin, Associate Professor
Chi-Hang Chan, Assistant Professor
Yanwei Jia, Assistant Professor
Yong Chen, Assistant Professor
Ka-Fai Un, Assistant Professor
Mo Huang, Assistant Professor
Ka-Meng Lei, Assistant Professor
Minglei Zhang, Assistant Professor
Yang Jiang, Assistant Professor
Wei-Han Yu, Assistant Professor

SKL-AMSV Administrative and Technical Staff

Fan Ng, Functional Head (Operation)
Un-Pang Lei, Functional Head (Technical)
Bin Zhou, Technology Transfer Officer
Chi-Wai Tang, Laboratory Technician- Safety Officer
Jie Gao, Laboratory Technician
Yuen-Ki Chan, Administrative Officer
Jianyu Zhong, Laboratory Technician
Pui-Wan Sou, Senior Administrative Assistant
Sut-Wai Ieong, Administrative Assistant

SKL-AMSV Scientific Advisory Board Members

Franco Maloberti, University of Pavia
Baher Haroun, Texas Instruments
Zhiliang Hong, Fudan University
Ming Liu, IME of Chinese Academy of Sciences
Howard Cam Luong, Hong Kong University of Science & Technology
Akira Matsuzawa, Tokyo Institute of Technology
Boris Murmann, Stanford University
Bram Nauta, University of Twente
Behzad Razavi, University of California, Los Angeles
Robert Bogdan Staszewski, University College Dublin
Zhihua Wang, Tsinghua University
Peter Chung-Yu Wu, Yang Ming Chiao Tung University
Hoi-Jun Yoo, Korea Advanced Institute of Science and Technology

Rui Paulo da Silva Martins
Vice Rector (Global Affairs), University of Macau
Chair Professor ECE, IEEE Fellow
Academician, Academy of Sciences of Lisbon, Portugal
Director, State Key Lab AMSV & Institute of Microelectronics

Rector's Office, N6-5033, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4309 | Email: RMartins@um.edu.mo

RESEARCH INTERESTS

Data Conversion and Signal Processing
Wireless IC
Biomedical IC
Integrated Power Electronics
Multidisciplinary Area of Microfluidics, Lab-on-a-Chip

PROFESSIONAL SERVICES

- Member, Advisory Board, Journal of Semiconductors, Chinese Institute of Electronics – CIE, Institute of Semiconductors, Chinese Academy of Sciences, 2021 - 2023
- Vice-Chair, IEEE CASS Fellow Evaluation Committee, Classes of 2021 & 2022
- General Chair, IEEE A-SSCC 2019
- Member, IEEE CASS Fellow Evaluation Committee, Class of 2019
- Chairman, IEEE CASS Fellow Evaluation Committee, Class of 2018
- General Chair, ACM/IEEE ASP-DAC 2016
- Nominations Committee Member, IEEE CAS Society 2016
- Division I (CASS, EDS, SSCS) – Director of IEEE, Nominating Committee, Representative of CASS, 2014
- IEEE CAS Society Fellow Evaluation Committee, Classes of 2013 & 2014
- Vice-President (World), Regional Activities and Membership of the IEEE CAS Society 2012-2013
- Associate Editor, IEEE TCAS-II 2010-2013
- Vice-President (Region 10/Asia, Australia, The Pacific) of the IEEE CAS Society 2009-2012
- General Chair, IEEE APCCAS 2008
- Founding Chairman, IEEE Macao Chapter CAS/COM, 2005-2008
- Founding Chairman, IEEE Macao Section, 2003-2005

AWARDS

- Macao Science & Technology Invention Awards (1st Prize) 2020, (2nd Prize) 2012, 2014, and 2016, 2020
- ISSCC 2018 - Takuo Sugano Award, 2018
- ASP-DAC 2018 - University LSI Design Contest Special Feature Award, 2018
- IEEE Council on Electronic Design Automation (CEDA) Outstanding Service Award 2016, Tokyo, Japan
- Business Awards of Macau – Innovation Excellence Award, 2014 (attributed to the SKL-AMSV)
- IEEE ISSCC Silk-Road Award 2011 and 2016 (as co-supervisor)
- IEEE Circuits and Systems Society "World-Chapter of the Year" 2009 (as Founding Chapter Chair)
- "Honorary Title of Value", Decoration attributed by the Macao Special Administrative Region Government (Chinese Administration), 2001
- "Medal of Merit (Class of Professional Merit)", Decoration attributed by the Macao Government (Portuguese Administration), 1999

THESIS SUPERVISED (OR CO-SUPERVISED)

26 Ph.D.

SELECTED PUBLICATIONS

- Rui P. Martins, Pui-In Mak, Sai-Weng Sin, et al., "Revisiting the Frontiers of Analog and Mixed-Signal Integrated Circuits Architectures and Techniques towards the future Internet of Everything (IoE) Applications", Foundations and Trends in Integrated Circuits and Systems, Now Publishers, Boston-Delft, in press, 2021 [Invited Paper]
- Rui P. Martins, Pui-In Mak, Chi-Hang Chan, Jun Yin, Yan Zhu, Yong Chen, Yan Lu, Man-Kay Law, Sai-Weng Sin, "Bird's-eye view of analog and mixed-signal chips for the 21st century", International Journal of Circuit Theory and Applications, Wiley Online Library, vol.49, pp.746-761, March 2021 [Invited Paper]
- Haoran Li, Ren Shen, Cheng Dong, Tianlan Chen, Yanwei Jia, Pui-In Mak, Rui P. Martins, "Turning on/off satellite droplet ejection for flexible sample delivery on digital microfluidics", Lab on a Chip, Royal Society of Chemistry, vol.20, pp.3709-3719, October 2020 [Inside Front Cover]
- Ren Shen, Yanwei Jia, Pui-In Mak, Rui P. Martins, "Clip-to-release on amplification (CRoA): a novel DNA amplification enhancer on and off microfluidics", Lab on a Chip, Royal Society of Chemistry, vol.20, pp.1928-1938, March 2020 [Outside Back Cover]
- Shiheng Yang, Jun Yin, Pui In Mak, R. P. Martins, "A 0.0056mm2 all-digital MDLL using edge re-extraction, dual-ring VCOs and a 0.3mW block-sharing frequency tracking loop achieving 292fsrmsJitter and −249dB FOM", IEEE International Solid - State Circuits Conference - (ISSCC), February 2018 [Invited Special Paper: "A 0.0056-mm2 -249-dB-FoM All-Digital MDLL using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs", IEEE Journal of Solid-State Circuits, vol.54, No.1, pp.88-98, January 2019]
- Yang Jiang, Man-Kay Law, Pui In Mak, R. P. Martins, "A 0.22-to-2.4V-Input Fine-Grained Fully-Integrated Rational Buck-Boost SC DC-DC Converter Using Algorithmic Voltage-Feed-In (AVFI) Topology Archiving 84.1% Peak Efficiency at 13.2μW/mm2", IEEE International Solid - State Circuits Conference - (ISSCC), February 2018 [Invited Special Paper: "Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters", IEEE Journal of Solid-State Circuits, vol.53, No.12, pp.3455-3469, December 2018]
- Mo Huang, Yan Lu, Seng-Pan U, R. P. Martins, A Reconfigurable Bidirectional Wireless Power Transceiver with Maximum Current Charging Mode and 58.6% Battery-to-Battery Efficiency, 2017 IEEE International Solid - State Circuits Conference - (ISSCC) [Takuo Sugano Award for Outstanding Far-East Paper 2018], February 2017] [Also published as: Mo Huang, Yan Lu, Rui P.Martins, "A Reconfigurable Bidirectional Wireless Power Transceiver for Battery-to-Battery Wireless Charging", IEEE Transactions on Power Electronics, vol.34, No.8, pp.7745-7753, August 2019]
- Ka-Meng Lei, Hadi Heidari, Pui-In Mak, Man-Kay Law, Franco Maloberti, Rui P.Martins, "A Handheld 50pM-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multy-Type Biological/Chemical Assays", IEEE International Solid-State Circuits Conference (ISSCC), February 2016 [Silk-Road Award for a Ph.D. Student from IEEE R-10]
- He-Gong Wei, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui P.Martins, Franco Maloberti, "A 0.024mm2 8-bit 400 MS/s SAR ADC with 2-bit/Cycle and Resistive DAC in 65 nm CMOS", IEEE International Solid-State Circuits Conference (ISSCC), February 2011 [Silk-Road Award for a Ph.D. Student from IEEE R-10]
- Yan Zhu, Chi-Hang Chan, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Rui P.Martins, Franco Maloberti, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS", IEEE Journal of Solid-State Circuits, vol.45, No.6, pp.1111-1121, June 2010 [Most cited journal paper of the SKLAB – 547 Citations in Google Scholar, October 2021]

Pui-In Mak (Elvis)
Professor, IEEE Fellow, IET Fellow, RSC Fellow
Chinese Academy of Sciences Overseas Expert
Deputy Director, State-Key Laboratory of Analog and Mixed-Signal VLSI
Deputy Director (Research), Institute of Microelectronics

Room 3006, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-8794 | Email: pimak@um.edu.mo

RESEARCH INTERESTS

4G/5G Cellular Transceivers (sub-6GHz, >28 GHz)
IoT Transceivers (Bluetooth LE, ZigBee)
Analog Techniques (amplifier, filter, crystal oscillator)
Portable In-Vitro Diagnostic Devices (DNA, Virus, proteins)
Microfluidic Technologies (digital, channel, hybrid)
Machine Learning Circuits (in-memory computing)

PROFESSIONAL SERVICES

- Chair of Distinguished Lecturer, IEEE CASS 2018-2019
- Distinguished Lecturer, IEEE SSCS 2017-2018
- Associate Editor, IEEE JSSC 2018-Present
- Associate Editor, IEEE SSCL 2017-Present
- Conference Chair, ICAC, 2019-2021
- TPC Member, IEEE ISSCC 2017-2019
- TPC Member, IEEE A-SSCC 2019
- TPC Member, IEEE ESSCIRC 2016-2017

AWARDS

- IEEE RFIC Best Student Paper Award'21
- Macao Science & Technology Invention Award – First Class '20
- Commemorative Medal, PRC's 70th Anniversary'19
- UM FST 30th Anniversary Outstanding Alumni Award'19
- IEEE APCCAS Best Paper Award'19

CURRENT GROUP MEMBERS

Ph.D.
Zhao Xianteng, 2017 (co-supervisor)
Guo Han, 2017 (co-supervisor)
Yang Zunsong, 2017 (co-supervisor)
Shao Haijun, 2018
Chen feifei, 2018
Meng Xi, 2018 (co-supervisor)
Xu Tailong, 2018 (co-supervisor)
Mao Jiaji, 2019 (co-supervisor)
Lin Liwen, 2019
Li Jixuan, 2019 (co-supervisor)
Tan Fei, 2020

SELECTED PUBLICATIONS

- G. Qi, H. Shao, P.-I. Mak, J. Y. and R. P. Martins, "A Multiband FDD SAW-less Transmitter for 5G-NR Using a BW-Extended N-Path Filter-Modulator, a Switched-BB Input and a Wideband TIA-Based PA Driver," IEEE Journal of Solid-State Circuits, vol. 55, pp. 3387-3399, Dec. 2020. [Also in ISSCC'20]

- S. Yang, J. Yin, H. Yi, W.-H. Yu, P.-I. Mak, R. P. Martins, "A 0.2-V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28nm CMOS," IEEE Journal of Solid-State Circuits, vol. 54, pp. 1351-1362, May 2019. [Also in ISSCC'18]

- S. Yang, J. Y., P.-I. Mak, R. P. Martins, "A 0.0056-mm2 −249-dB-FOM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring-VCOs," IEEE Journal of Solid-State Circuits, vol. 54, pp. 88-98, Jan. 2019. [Also in ISSCC'18]

- C.-C. Lim, H. Ramiah, J. Yin, P.-I. Mak, R. P. Martins, "An Inverse-Class-F CMOS Oscillator with Intrinsic-High-Q 1st-Harmonic and 2nd-Harmonic Resonances," IEEE Journal of Solid-State Circuits, vol. 53, pp. 3528-3539, Dec. 2018. [Also in ISSCC'18]

- K.-M. Lei, P.-I. Mak, M.-K. Law, R. P. Martins, "A Regulation-Free Sub-0.5 V 16/24-MHz Crystal Oscillator with 14.2-nJ Startup Energy and 31.8-µW Steady-State Power," IEEE Journal of Solid-State Circuits, vol. 53, pp. 2624-2635 , Sept. 2018. [Also in ISSCC'18]

- H. Yi, W.-H. Yu, P.-I. Mak, J. Yin, R. P. Martins, "A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver Front-End with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS," IEEE Journal of Solid-State Circuits, vol. 53, pp. 1618-1627, Jun. 2018. [Also in ISSCC'17]

- G. Qi, B. Liempd, P.-I. Mak, R. P. Martins, J. Craninckx, "A SAW-Less Tunable RF Front-End for FDD and IBFD Combining an Electrical-Balance Duplexer and a Switched-LC N-Path LNA," IEEE Journal of Solid-State Circuits, vol. 53, pp. 1431-1442, May 2018.

Sai-Weng Sin (Terry)
Associate Professor, IEEE Senior Member
Associate Director (Academic), State-Key Laboratory of Analog and Mixed-Signal VLSI
Deputy Director (Academic), Institute of Microelectronics

Room 3007, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-8795 | Email: terryssw@um.edu.mo

RESEARCH INTERESTS

High-Performance Data Converters
- Nyquist Data Converters
- Oversampling Data Converters

Power Management Integrated Circuits
Analog and Mixed-Signal Integrated Circuits
Analog Integrated Circuits for Artificial Intelligence

PROFESSIONAL SERVICES

- TPC Member, A-SSCC 2013-Present
- SDC Member, A-SSCC 2013-Present
- RCM Member, ISCAS 2017-Present
- Subcommittee Chair, ICTA 2018-Present
- Associate Editor, IEEE Transactions on Circuits and Systems II – Express Briefs
- Associate Editor, IEEE Access
- Editorial Board Member, MDPI Electronics
- Secretary, IEEE Solid-State Circuit Society (SSCS) Macau Chapter, 2009-2016
- Treasurer/Secretary, IEEE Macau CAS/COM Joint Chapter, 2009-2016
- Treasurer (Local Organization Committee), A-SSCC, 2019

AWARDS

- National Scientific & Technological Progress Award'11
- Macao Science & Technology Special Awards'12
- Macao Science & Technology Invention Awards'12'14'16'20
- IEEE ISSCC Silkroad Award'11
- IEEE SSCS Pre-Doctoral Achievement Award 2015 (as advisor)
- IEEE CASS Scholarship Award 2017 (as advisor)
- IEEE A-SSCC Best Student Design Contest Award'11 (as advisor)
- IEEE ICTA Best Paper Award'19
- IEEE ASICON Best Student Paper Award'19 (as advisor)

CURRENT GROUP MEMBERS

Ph.D.
Dongyang Jiang, 2014
Chengzhe Liu, 2019
Ke Li, 2019
Ran Zhang, 2019
Haoyu Gong, 2020
Xueru Cen, 2020
Yang Lu, 2020

M.Sc.
Song Cui, 2016
Qingyu Ma, 2017
Shulin Zhao, 2018

POST-DOC./R.A.
Mingqiang Guo, 2020

SELECTED PUBLICATIONS

- D. Jiang, L. Qi, S.-W. Sin, F. Maloberti, R.P.Martins, "A Time-Interleaved 2nd-order ΔΣ Modulator Achieving 5 MHz Bandwidth and 86.1dB SNDR Using Digital Feedforward Extrapolation," in press in IEEE Journal of Solid-State Circuits [Also in VLSI'20].

- M. Guo, J. Mao, S.-W. Sin, H. Wei, R.P.Martins, "A 1.6GS/s 12.2mW 7/8-way Split Time-Interleaved SAR ADC achieving 54.2-dB SNDR with Digital Background Timing Mismatch Calibration," in IEEE Journal of Solid-State Circuits, vol. 55, Issue 3, pp. 693-705, Mar 2020 [invited special issue of CICC'19].

- L. Qi, A. Jain, D. Jiang, S.-W. Sin, R. P. Martins and M. Ortmanns, "A 76.6dB-SNDR 50MHz-BW 29.2mW Multibit CT Sturdy MASH with DAC Non-Linearity Tolerance," in IEEE Journal of Solid-State Circuits, vol. 55, Issue 2, pp. 344-355, Mar 2020 [Also in ISSCC'19].

- U. Chio, K.-C. Wen, S.-W. Sin, C.-S. Lam, Y. Lu, F. Maloberti, R. P. Martins, " An Integrated DC-DC Converter with Segmented Frequency Modulation and Multiphase Co-Work Control for Fast Transient Recovery", in IEEE Journal of Solid-State Circuits, vol. 54, Issue 10, pp. 2637-2648, Oct 2019 [Invited Special Issue of A-SSCC'18].

- B. Wang, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, "A 550μW 20kHz BW 100.8dB SNDR Linear-Exponential Multi-Bit Incremental ΣΔ ADC with 256 clock cycles in 65nm CMOS", in IEEE Journal of Solid-State Circuits, vol. 54, Issue 4, pp. 1161-1172, Apr 2019 [Invited Special Issue of VLSI'18].

Man-Kay Law (Matthew)
Associate Professor, IEEE Senior Member
Laboratory Infrastructure Coordinator, Institute of Microelectronics

Room 4027, 4/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-8791 | Email: mklaw@um.edu.mo

RESEARCH INTERESTS

CMOS Image Sensor
CMOS Temperature Sensor
Analog Techniques/Sensor Interface Circuits
Voltage/Current References
Energy Harvesting Circuits and Systems

PROFESSIONAL SERVICES

- Distinguished Lecturer, SSCS, 2019-2021
- Distinguished Lecturer, CASS, 2018-2021
- Guest Editor, IEEE JSSC, 2021
- Guest Editor, IEEE Access, 2020
- TPC Member, IEEE ISSCC 2018-Present
- TPC Member, IEEE ASP-DAC 2016
- TC Member, IEEE CASS SSTC, 2012-Present
- TC Member, IEEE CASS BioCAS TC, 2012-Present
- RC Member, IEEE ISCAS, 2012-Present

AWARDS

- Macau FDCT Technology Invention Award, 1st Class, '20
- Macau FDCT Technology Invention Award, 2nd Class, '14'18
- Invited Keynote Speaker, IEEE ICTA'20
- IEEE SSCS Pre-Doctoral Achievement Awards'18 (as advisor)
- IEEE ISSCC Silkroad Award'16 (as advisor)
- IEEE ASPDAC Best Design Award'16
- IEEE A-SSCC Distinguished Design Award'15
- IEEE ISQED, Student Paper Award'13 (as advisor)

CURRENT GROUP MEMBERS

Ph.D.
Li Meng, 2020
Chongyao Xu, 2019
Guangshu Zhao, 2019
Chi-Wah U, 2019 (co-supervisor)
Jiangchao Wu, 2016
Xin Lu, 2016

M.Sc.
Yangyang Liu, 2019
Yu Lei, 2019
Jieyun Zhang, 2018

POST-DOC./R.A.
Chao Xie, 2020

SELECTED PUBLICATIONS

- Z. Chen, M. K. Law, P. I. Mak, X. Zeng and R. P. Martins, "Piezoelectric Energy Harvesting Interface using Split-Phase Flipping-Capacitor Rectifier with Capacitor-Reuse for Input Power Adaptation," IEEE J. Solid-State Circuits, vol. 55, no. 8, pp. 2106-2117, Aug. 2020. [Also in ISSCC 2019]

- Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter With Wide Input Voltage Range and Enhanced Power Density," IEEE J. Solid-State Circuits, vol. 54, no. 11, pp. 3118-3134, Nov. 2019.

- Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters," IEEE J. Solid-State Circuits, vol. 53, no. 12, pp. 3455-3469, Dec. 2018. [Also in ISSCC'18]

- Z. Chen, M. K. Law, P. I. Mak, W. H. Ki and R. P. Martins, "Fully-Integrated Inductor-less Flipping-Capacitor Rectifier (FCR) for Piezoelectric Energy Harvesting," IEEE J. Solid-State Circuits, vol. 52, no. 12, pp. 3168-3180, Dec. 2017. [Also in ISSCC'17]

- Xin Lu, Man-Kay Law, Yang Jiang, Xiaojin Zhao, Pui-In Mak and Rui P. Martins, "A 4μm Diameter SPAD Using Less-doped N-Well Guard Ring in Baseline 65nm CMOS," IEEE Transactions on Electron Devices, vol. 67, pp. 2223-2225, May 2020.

Yan Zhu (Julia)
Associate Professor, IEEE Senior Member
Industrial Collaboration Coordinator, Institute of Microelectronics

Room 4023, 4/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4418 | Email: yanzhu@um.edu.mo

RESEARCH INTERESTS

High-Speed ADCs
ADC Buffer
ADC LDO and Reference Buffer
ADC Calibration
Noise-shaping SAR ADCs
Hybrid ADCs
Mixed-Signal Circuits

PROFESSIONAL SERVICES

- Reviewer of IEEE JSSC, SSCL, TCAS-I, TCAS-II, TVLSI, Access, etc. TPC of ISSCC and A-SSCC

CURRENT GROUP MEMBERS

Ph.D.
Buhui Rui
Lai Wei
Zihao Zheng
Zixuan Xu
Xianghui Pan
Yu Duan
Junlin Zhong
Jiahao Liu

M.Sc.
Yaozhong Ou
Yi Zeng

POST-DOC./R.A.
Jiang Wenning
Yanbo Zhang
Junyan Hao
Zhang Yanna
Zhang Hongzhi

SELECTED PUBLICATIONS

- Z. Zheng et al., "16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation," 2020 IEEE International Solid - State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 254-256.

- M. Zhang, Y. Zhu, C. H. Chan, and R. P. Martins, "A 8-bit 10-GS/s 16× interpolation-based time-domain ADC with <1.5-ps uncalibrated quantization steps," IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3225-3235, Dec. 2020.

- Y. Song, Y. Zhu, C. H. Chan and R. P. Martins, "9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 164-166.

- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 0.6-V 13-bit 20-MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed enhanced techniques," IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3396-3408, Dec. 2019.

- X. Yang, C. Chan, Y. Zhu and R. P. Martins, "16.3 A −246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 260-262.

- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 4× interleaved 10GS/s 8b time-domain ADC with 16× interpolation-based inter-stage gain achieving >37.5dB SNDR at 18GHz input," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2020, pp. 252-253.

- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 0.6V 13b 20MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed enhanced techniques," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2019, pp. 66-67.

- W. Jiang, Y. Zhu, M. Zhang, C. Chan and R. P. Martins, "3.2 A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 60-62.

Yan Lu
Associate Professor, IEEE Senior Member
Microelectronics Research Center/ZUMRI Coordinator,
Institute of Microelectronics
Member, Microelectronics Education Committee,
Institute of Microelectronics

Room 3014, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4408 | Email: yanlu@um.edu.mo

RESEARCH INTERESTS

Wireless Power Transfer Systems and Circuits
Highly-Integrated DC-DC Power Converters
Linear Voltage Regulators
Energy Harvesting Circuits (RF and Solar)

PROFESSIONAL SERVICES

- Young Editor, Journal of Semiconductor 2021-2023
- Guest Editor, IEEE TCAS-I 2019
- Guest Editor, IEEE TCAS-II 2018 and 2019
- Co-Founder, Workshop on IC Advances in China (ICAC)
- Steering Committee Member, IEEE ICTA 2020-Present
- TPC Member, IEEE ISSCC 2019-Present
- TPC Member, IEEE CICC 2019-Present
- TPC Member, IEEE ISCAS 2016-2020

AWARDS

- Macao S&T Invention Awards 2nd Prize 2018 and 2020
- IEEE ISSCC Outstanding Far-East Paper 2017
- IEEE CASS Outstanding Young Author Award 2017
- IEEE SSCS Pre-Doctoral Achievement Award 2013-14
- PSMA PwrSoC Best Student Poster 1st Prize (as Advisor) 2018

CURRENT GROUP MEMBERS

Ph.D.
Guigang Cai, 2017
Xianglong Bai, 2017 (UM-SUSTech Joint Program)
Shuangxing Zhao, 2017 (UM-SUSTech Joint Program)
Chengyu Huang, 2018 (UM-SUSTech Joint Program)
Junwei Huang, 2018 (co-supervisor)
Yifan Jiang, 2019
Xiangyu Mao, 2019
Yang Li, 2021
Zhiguo Tong, 2021

M.Sc.
Han Yin, 2018
Shengnan Zhou, 2019
Zixiao Lin, 2019
Nan Shi, 2021

POST-DOC./R.A.
Chuang Wang, 2018
Fangyu Mao, 2020
Xiaofei Li, 2021

SELECTED PUBLICATIONS

- J. Lin, Y. Lu, C. Zhan, and R. P. Martins, "A Single-Stage Dual-Output Regulating Rectifier with Hysteretic Current-Wave Modulation," IEEE Journal of Solid-State Circuits, early access online.
- F. Mao, Y. Lu, E. Bonizzoni, F. Boera, M. Huang, F. Maloberti, and R. P Martins, "A Hybrid Single-Inductor Bipolar-Output DC-DC Converter With Floating Negative Output for AMOLED Displays," IEEE Journal of Solid-State Circuits, early access online.
- X. Li, F. Mao, Y. Lu, and R. P. Martins, "A VHF Wide-Input Range CMOS Passive Rectifier With Active Bias Tuning," IEEE Journal of Solid-State Circuits, vol. 55, no. 10, pp. 2629–2638, Oct. 2020.
- F. Mao, Y. Lu, and R. P. Martins, "A Reconfigurable Cross-Connected Wireless-Power Transceiver for Bidirectional Device-to-Device Wireless Charging," IEEE Journal of Solid-State Circuits (JSSC), vol. 54, no. 9, pp. 2579-2589, Sep. 2019. [Also in ISSCC 2018]
- M. Huang, Y. Lu, and R. P. Martins, "A Reconfigurable Bidirectional Wireless Power Transceiver for Battery-to-Battery Wireless Charging," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7745–7753, Aug. 2019. [Also in ISSCC 2017]
- G. Cai, Y. Lu, C. Zhan, and R. P. Martins, "A Fully Integrated FVF LDO With Enhanced Full-Spectrum Power Supply Rejection," IEEE Transactions on Power Electronics, vol. 36, no. 4, pp. 4326–4337, Apr. 2021.
- Y. Lu, M. Huang, and R. P. Martins, "PID Control Considerations for Analog-Digital Hybrid Low-Dropout Regulators," in IEEE International Conference on Electron Devices and Solid-State Circuits (EDSSC), Jun. 2019.

Vai Mang I
Associate Professor
IEEE Senior Member

Room 3035, 3/F, E11, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4461 | Email: fstmiv@um.edu.mo

RESEARCH INTERESTS

Optrode (electronics circuits)
Neural Spiking Network (hardware implementation, algorithms)
CMUT (transducer design and modeling, front end, imaging)
Embedded Systms (RTOS, multi-tasking)

PROFESSIONAL SERVICES

- Board Member, CBME 2016-2021
- President, MSBME 2009-2021
- Advisor, IEEE Macau, 2013-2021
- Board Member, IEEE EMBS Hong Kong - Macau Joint Chapter, 2013-2021
- Board Member, **中國生物醫學工程學會神經醫學工程分會委員會**, 2014-2021
- Board Member, **中國電子學會生物醫學電子學分會**, 2003-2021
- Board Member, **中國電子學會信息論分會**, 2008-2021
- **評審委員**, **全国青少年科技创新大赛**, 2017-2018
- Chair, **澳門城市總體規劃諮詢文本交流會**, 2020
- Invited Keynote Speaker, **人体机能实验教学研讨会**, 2021
- Invited Speaker, **浙江大学西湖学术论坛**, 2019
- Invited Speech, SUST, 2018
- TPC Member, 2020 International Conference on Medical Material and Chemical Engineering
- Invited Speech, Guilin University of Electronic Technology, 2020
- Reviewer, IEEE UFFC outstanding paper 2016-2019

AWARDS

- **优秀创新创业导师**, **第五届中国“互联网+”大学生创新创业大赛**, 2019

CURRENT GROUP MEMBERS

Ph.D.
ALI SIDDIQUE, 2019
LIU SHUAIQI, 2018
WANG PANKE, 2015
WANG JIUJIANG, 2012
ZHANG SHUANG, 2011

M.Sc.
MA XIANGXI, 2021
FAN SHAOCAN, 2017
ZHAN YI, 2017

POST-DOC./R.A.
YU YUANYU, 2019

SELECTED PUBLICATIONS

- H Wu, Y Gao, J Yang, M Vai, M Du, S Pun, “Development of a Photoelectric Adjustment System With Extended Range for Fluorescence Immunochromatographic Assay Strip Readers,” IEEE Photonics Journal, vol. 13, Jun. 2021.
- X Yang, P Sun, J Wu, W Jiang, M Vai, S Pun, C Peng, F Chen, “Nondestructive and objective assessment of the vestibular function in rodent models: A review,” Neuroscience letters, vol. 717, pp. 134608, Jan, 2020.
- L Shao, S Liu, S Bandyopadhyay, F Yu, W Xu, C Wang, H Li, M Vai, L Du, J Zhang, “Data-driven distributed optical vibration sensors: a review,” IEEE Sensors Journal, vol. 20, pp. 6224-6239, Sep. 2019.
- P Sun, Y Zhang, F Zhao, J Wu, S Pun, C Peng, M Du, M Vai, D Liu, F Chen, “An assay for systematically quantifying the vestibulo-ocular reflex to assess vestibular function in zebrafish larvae,” vol. 12, Aug, 2018.
- X Chen, S Barma, S Pun, M Vai, P Mak, “Direct measurement of elbow joint angle using galvanic couple system,” IEEE Transactions on Instrumentation and Measurement, vol. 66, Feb, 2017.

Sio Hang Pun (Lodge)
Associate Professor, , IEEE Senior Member
Member, Microelectronics Education Committee,
Institute of Microelectronics

Room 3013, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4467 | Email: lodgepun@@um.edu.mo

RESEARCH INTERESTS

Biomedical electronics
Neuroscience application
Capacitive Micro-machined Ultrasonic Transducers
Bio-electromagnetism
Intra-body communication

PROFESSIONAL SERVICES

- Chair, IEEE Engineering on Biology and Medicine Engineering Society (EMBS) Hong Kong and Macau Joint Chapter, 2013
- Executive Committee member, IEEE Engineering on Biology and Medicine Engineering Society (EMBS) Hong Kong and Macau Joint Chapter, 2012-Present
- Member, Asia-Pacific work group, International Federation of Medical and Biological Engineering (IFMBE), 2019-present
- Member, APCMBE steering committee (International organization committee), 2020
- Reviewer, IEEE Transaction on Biomedical Engineering
- Reviewer, IEEE Transactions on Ultrasonic, Ferroelectric, and Frequency Control
- Reviewer, IEEE Journal on Biomedical and Health Informatics
- Reviewer, IEEE Engineering on Biology and Medicine Engineering Conference (EMBC), 2009-Present

AWARDS

- Invited Keynote Speaker, ICQCA 2021: International Conference on Quantum Computing and Algorithms

CURRENT GROUP MEMBERS

Ph.D.
Benzheng Li, 2017
Cheng Li, 2017
Mingtao Li, 2018
Ali Siddique, 2019 (co-supervisor)
WeiHao Lin, 2019 (co-supervisor)
Peng Sun, 2017 (co-supervisor)

M.Sc.
JieYu Ma, 2020
Hong Liang Loo, 2020
U Tok Cheong, 2019
U Kin Che, 2017
LiYang Wang, 2017

POST-DOC./R.A.
ChangHao Chen 2019
YuanYu Yu, 2020
JiuJiang Wang, 2020

SELECTED PUBLICATIONS

- H.Wu et al., "Development of a Photoelectric Adjustment System With Extended Range for Fluorescence Immunochromatographic Assay Strip Readers," IEEE Photonics J., vol. 13, no. 3, pp. 1–12, 2021.
- Y.Yu et al., "Experimental Characterization of an Embossed Capacitive Micromachined Ultrasonic Transducer Cell," Micromachines, vol. 11, no. 2, p. 217, Feb.2020, 10.3390/mi11020217.
- P. K.Wang et al., "Low-latency single channel real-time neural spike sorting system based on template matching," PLoS One, vol. 14, no. 11, p. e0225138, 2019.
- S.Zhang et al., "Experimental Verifications of Low Frequency Path Gain (PG) Channel Modeling for Implantable Medical Device (IMD)," IEEE Access, vol.7 , pp. 11934–11945, 2019, 10.1109/ACCESS.2019.2892130.
- Z. Mohammadi et al., "Computationally inexpensive enhanced growing neural gas algorithm for real-time adaptive neural spike clustering," J. Neural Eng., vol. 16, no. 5, pp. 1–18, 2019, 10.1088/1741-2552/ab208c.
- S. H.Pun et al., "Monolithic Multiband CMUTs for Photoacoustic Computed Tomography with In Vivo Biological Tissue Imaging," IEEE Trans. Ultrason. Ferroelectr. Freq. Control, vol. 65, no. 3, pp. 465–475, 2018.
- Y.Yu et al., "Design of a Collapse-Mode CMUT with an Embossed Membrane for Improving Output Pressure," IEEE Trans. Ultrason. Ferroelectr. Freq. Control, 2016, 10.1109/TUFFC.2016.2554612.
- C. H.Chen et al., "An Integrated Circuit for Simultaneous Extracellular Electrophysiology Recording and Optogenetic Neural Manipulation," IEEE Trans. Biomed. Eng., vol. 64, no. 3, pp. 557–568, 2017, 10.1109/TBME.2016.2609412.

Chi-Seng Lam (Terence)
Associate Professor, IEEE Senior Member
Member, Microelectronics Education Committee,
Institute of Microelectronics

Room 3012, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4417 | Email: cslam@um.edu.mo

RESEARCH INTERESTS

Power Management Integrated Circuits
Wireless Power Transfer
Power Converters
Power Quality Compensators
Renewable Energy Generation Systems

PROFESSIONAL SERVICES

- Vice-Chair, IEEE Macau Section 2016-2020
- Chair, IEEE Macau IES Chapter 2019-Present
- Chair, IEEE Macau CAS & COM Joint Chapter 2017-2018
- Vice-Chair, IEEE Macau PES & PELS Chapter 2020-Present
- Associate Editor, IEEE TIE 2020-Present
- Associate Editor, IEEE OJES 2020-Present
- Associate Editor, IEEE Access 2020-Present
- Guest Editor, IEEE TCAS-II 2020-2021
- Guest Editor, IET PEL 2020-2021
- Tutorial Speaker, IEEE ISCAS 2021
- Tutorial Speaker, IEEE IECON 2020
- Tutorial Speaker, IEEE APPEEC 2019
- Chair, IEEE IES PETC Power Quality Subcommittee 2020-Present
- TC Member, IEEE IES ESOC 2019-Present
- TC Member, IEEE IES RES 2019-Present
- TC Member, IEEE CAS PECAS 2019-Present

AWARDS

- Macao Science & Technology Invention Awards'14'18
- IEEE PES Chapter Outstanding Engineer Award'17
- Best Track Paper Award, IEEE PES APPEEC'19
- Best Paper Award, IEEE ICTA'19
- Macao Science & Technology Award for Postgraduates' 12
- IIM Young Research Award'20 (as advisor)
- Silver Award, The 6th China International University Students' "Internet +" Innovation and Entrepreneurship Competition (as advisor)

CURRENT GROUP MEMBERS

Ph.D.
Cheng Gong, 2018
Junwei Huang, 2018
Wai-Kit Sou, 2019
Chi-Wa U, 2019
Caolei Pan, 2019
Io-Wa Iam, 2020

M.Sc.
Sibo Wen, 2019
Lei Xuan, 2019
Iok-U Hoi, 2020
Cong Liu, 2020
Chio-Kuan Choi, 2020

POST-DOC./R.A.
Wen-Liang Zeng, 2020

SELECTED PUBLICATIONS

- Zhicong Huang, Chi-Seng Lam, Pui-In Mak, Rui P. Martins, Siu-Chung Wong, and Chi K. Tse, "A single-stage inductive-power-transfer converter for constant-power and maximum-efficiency battery charging" IEEE Transactions on Power Electronics (TPEL), vol. 35, no. 9, pp. 8973 – 8984, Sept. 2020.

- Wen-Liang Zeng, Yuan Ren, Chi-Seng Lam, Sai-Weng Sin, Weng-Keong Che, Ran Ding, Rui P. Martins, "A 470-nA quiescent current and 92.7%/94.7% efficiency DCT/PWM control buck converter with seamless mode selection for IoT application", IEEE Transactions on Circuits and Systems I - Regular Papers (TCAS-I), vol. 67, no. 11, pp. 4085 – 4098, Nov. 2020.

- Wen-Liang Zeng, Chi-Seng Lam, Sai-Weng Sin, Franco Maloberti, Man-Chung Wong, Rui P. Martins, "A 220-MHZ bondwire-based fully-integrated KY converter with fast transient response under DCM operation", IEEE Transactions on Circuits and Systems I - Regular Papers (TCAS-I), vol. 65, no. 11, pp. 3984 – 3995, Nov. 2018.

- Lei Wang, Chi-Seng Lam, Man-Chung Wong, "Analysis, control, and design of a hybrid grid-connected inverter for renewable energy generation with power quality conditioning", IEEE Transactions on Power Electronics (TPEL), vol. 33, no. 8, pp. 6755 – 6768, Aug. 2018.

- Chi-Seng Lam, Lei Wang, Sut-Ian Ho, Man-Chung Wong, "Adaptive thyristor controlled LC – hybrid active power filter for reactive power and current harmonics compensation with switching loss reduction," IEEE Transactions on Power Electronics (TPEL), vol. 32, no. 10, pp. 7577 – 7590, Oct. 2017.

Jun Yin (Kevin)
Associate Professor, IEEE Member
Member, Industrial Collaboration and Microelectronics Center/ZUMRI, Institute of Microelectronics

Room 4027, 4/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4407 | Email: junyin@um.edu.mo

RESEARCH INTERESTS

Frequency Generation Circuits
Low-Power Wireless Transceivers for IoT Application

PROFESSIONAL SERVICES

- Associate Editor, IEEE TCAS-I 2020-Present
- Associate Editor, ELSEVIER Integration the VLSI Journal
- TPC Member, IEEE ISSCC 2022-Present
- TPC Member, IEEE ESSCIRC 2020-Present
- TPC Member, IEEE A-SSCC 2019, 2021-Present
- TPC Member, IEEE ISCAS 2017-Present
- TPC Member, IEEE ICTA 2019-Present

AWARDS

- Macao Science & Technology Invention Awards'18'20
- IEEE SSCS Pre-Doctoral Achievement Awards '19 (as advisor)
- IEEE CICC Student Scholarship Award'12

CURRENT GROUP MEMBERS

Ph.D.
Xi Meng, 2018
Jiaji Mao, 2019
Tailong Xu, 2019
Zhizhan Yang, 2019
Xiaoqi Lin, 2019
Jiang Yang, 2019
Xiangxun Zhan, 2020
Haoran Li, 2020
Qiyao Jiang, 2020

M.Sc.
Bolun Su, 2018
Shenke Zhong, 2019
Tianxiao Xie, 2019

SELECTED PUBLICATIONS

- C. Fan, J. Yin, C. -C. Lim, P. -I. Mak, and R. P. Martins, "A 9mW 54.9-to-63.5GHz Current-Reuse LO Generator with a 186.7dBc/Hz FoM by Unifying a 20GHz 3rd-Harmonic-Rich Current-Output VCO, a Harmonic-Current Filter and a 60GHz TIA," IEEE International Solid-State Circuit Conference (ISSCC), Feb. 2020.

- S. Yang, J. Yin, H. Yi, W. -H. Yu, P. -I. Mak, and R. P. Martins, "A 0.2-V Energy-Harvesting BLE Transmitter with a Micropower Manager Achieving 25% System Efficiency at 0-dBm Output and 5.2-nW Sleep Power in 28-nm CMOS," IEEE Journal of Solid-State Circuits (JSSC), vol. 54, May. 2019. [Also in ISSCC 2018]

- S. Yang, J. Yin, P. -I. Mak, and R. P. Martins, "A 0.0056-mm² -249-dB-FoM All-Digital MDLL Using a Block-Sharing Offset-Free Frequency-Tracking Loop and Dual Multiplexed-Ring VCOs," IEEE Journal of Solid-State Circuits (JSSC), vol. 54, Jan. 2019. [Also in ISSCC 2018]

- C. -C. Lim, H. Ramiah, J. Yin, P. –I. Mak, and R. P. Martins, "An Inverse-Class-F CMOS Oscillator With Intrinsic-High-Q First Harmonic and Second Harmonic Resonances," IEEE Journal of Solid-State Circuits (JSSC), vol. 53, Dec. 2018. [Also in ISSCC 2018]

- Y. Peng, J. Yin, P. -I. Mak, and R. P. Martins, "Low-Phase-Noise Wideband Mode-Switching Quad-Core-Coupled mm-wave VCO Using a Single-Center-Tapped Switched Inductor," IEEE Journal of Solid-State Circuits (JSSC), vol. 53, Nov. 2018.

- X. Peng, J. Yin, P. -I. Mak, W. -H. Yu, and R. P. Martins, "A 2.4-GHz ZigBee Transmitter Using a Function-Reuse Class-F DCO-PA and an ADPLL Achieving 22.6% (14.5%) System Efficiency at 6-dBm (0-dBm) Pout," IEEE Journal of Solid-State Circuits (JSSC), vol. 52, Jun. 2017.

- J. Yin, P.-I. Mak, F. Maloberti, and R. P. Martins, "A Time-Interleaved Ring-VCO with Reduced 1/f³ Phase Noise Corner, Extended Tuning Range and Inherent Divided Output," IEEE Journal of Solid-State Circuits (JSSC), vol. 51, Dec. 2016. [Also in ISSCC 2016]

Chi-Hang Chan (Ivor)
Assistant Professor, IEEE Member
Member, Industrial Collaboration and Microelectronics Center/ZUMRI, Institute of Microelectronics

Room 4023, 4/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4402 | Email: ivorchan@um.edu.mo

RESEARCH INTERESTS

Noise-shaping SAR ADCs
Wideband Sigma Delta Modulators
Low Jitter Ring-VCO-based PLL
High-Speed ADCs
Hybrid ADCs
Mixed-Signal Circuits
Time-Domain Integrated Circuits

PROFESSIONAL SERVICES

- Reviewer of IEEE JSSC, SSCL, TCAS-I, TCAS-II, TVLSI, Access, etc.

CURRENT GROUP MEMBERS

- **Ph.D.**
  Kai Xing
  Hongshuai Zhang
  Zehang Wu
  Yuanzhe Zhao
- **M.Sc.**
  Sifan Wang
  Chaorui Zou
- **POST-DOC./R.A.**
  Jiang Wenning
  Yanbo Zhang
  Junyan Hao
  Zhang Yanna
  Zhang Hongzhi

SELECTED PUBLICATIONS

- Z. Zheng et al., "16.3 A Single-Channel 5.5mW 3.3GS/s 6b Fully Dynamic Pipelined ADC with Post-Amplification Residue Generation," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 254-256.
- M. Zhang, Y. Zhu, C. H. Chan, and R. P. Martins, "A 8-bit 10-GS/s 16× interpolation-based time-domain ADC with <1.5-ps uncalibrated quantization steps," IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3225-3235, Dec. 2020.
- Y. Song, Y. Zhu, C. H. Chan and R. P. Martins, "9.6 A 2.56mW 40MHz-Bandwidth 75dB-SNDR Partial-Interleaving SAR-Assisted NS Pipeline ADC With Background Inter-Stage Offset Calibration," 2020 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2020, pp. 164-166.
- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 0.6-V 13-bit 20-MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed enhanced techniques," IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3396-3408, Dec. 2019.
- X. Yang, C. Chan, Y. Zhu and R. P. Martins, "16.3 A −246dB Jitter-FoM 2.4GHz Calibration-Free Ring-Oscillator PLL Achieving 9% Jitter Variation Over PVT," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 260-262.
- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 4× interleaved 10GS/s 8b time-domain ADC with 16× interpolation-based inter-stage gain achieving >37.5dB SNDR at 18GHz input," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2020, pp. 252-253.
- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 0.6V 13b 20MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed enhanced techniques," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2019, pp. 66-67.
- W. Jiang, Y. Zhu, M. Zhang, C. Chan and R. P. Martins, "3.2 A 7.6mW 1GS/s 60dB SNDR Single-Channel SAR-Assisted Pipelined ADC with Temperature-Compensated Dynamic Gm-R-Based Amplifier," 2019 IEEE International Solid- State Circuits Conference - (ISSCC), San Francisco, CA, USA, 2019, pp. 60-62.

Yanwei Jia
Assistant Professor
Member, Lab Infrastructure and Testing Facilities Committee, Institute of Microelectronics

Room 3001a, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4451 | Email: yanweijia@um.edu.mo

RESEARCH INTERESTS

Digital Microfluidics Technology development
Novel Techniques for Disease Diagnostics
Digital Microfluidics for Precision Medicine
Drug Screening in Digital Microfluidics

PROFESSIONAL SERVICES

- Reviewers for the prestigious journals:
- Lab on a Chip
- Chemical Science
- ACS Applied Materials and Interfaces
- ACS Sensors
- Analytical Chemistry
- ChemComm
- Talanta
- Langmuir
- Micromachines
- Biomicrofluidics
- Microchimica Acta
- Microfluidics and Nanofluidics
- Rection Chemistry and Engineering
- Sensors

AWARDS

- Innovation Award, The 9th International Multidisciplinary Conference on Optofluidics, 2019

GRADUATED STUDENTS

Ph.D.
Ren Shen, 2021
Haoran Li, 2021

M.Sc.
Yujun Mao, 2021

CURRENT GROUP MEMBERS

Ph.D.
Liang Wan
Sizhe Dong
Bingyang Ye

M.Sc.
Wenjun Miao

POST-DOC./R.A.
Xiaojun Chen
Meiqing Liu
Yingying Liu
Caiwei Li

SELECTED PUBLICATIONS

- H. R. Li, R. Shen, Y. W. Jia*, P. I. Mak, R. P. Martins, Turning on/off satellite droplet ejection for flexible sample delivery on digital microfluidics, Lab on a Chip, 20,3709-3719, 2020 (Inside Front Cover).
- R. Shen, Y. W. Jia*, P. I. Mak, and R. P. Martins, Clip to release on amplification (CRoA): a novel enhancer for DNA amplification on and off microfluidics, Lab on a Chip, 20, 1928-1938, 2020 (Outside Back Cover).
- J. Zhai, H. R. Li, A. H. H. Wong, C. Dong, S. H. Yi, Y. W. Jia*, P. I. Mak, C. X. Deng and R. P. Martins, A digital microfluidic system with 3D microstructures for single-cell culture, Microsystems and Nanoengineering, 6, 6, 2020.
- J. Zhai, S. H. Yi, Y. W. Jia*, P. I. Mak, R. P. Martins, Cell-based drug screening on microfluidics, Trends in Analytical Chemistry, 117, 231-241, 2019.
- M. Z. Li, C. Dong, M. K. Law*, Y. W. Jia*, P. I. Mak and R. P. Martins, Hydrodynamic-flow-enhanced rapid mixer for isothermal DNA hybridization kinetics analysis on digital microfluidics platform, Sensors and Actuators B, 287, 390-397, 2019.
- C. Dong, Y. W. Jia*, J. Gao, T. L. Chen, P. I. Mak, M. I. Vai and R. P. Martins, A 3D microblade structure for precise and parallel droplet splitting on digital microfluidic chips, Lab on a Chip, 17, 896-904, 2017.

Yong Chen (Nick)
Assistant Professor, IEEE Senior Member
Member, Industrial Collaboration and Microelectronics Center/ZUMRI, Institute of Microelectronics

Room 3015g, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4470 | Email: ychen@um.edu.mo

RESEARCH INTERESTS

High-speed wireline communication for electrical and optical interconnects
RF/mm-wave/sub-THz communication systems and circuits
Analog/mixed-signal CMOS integrated circuits

PROFESSIONAL SERVICES

- Associate Editor of IEEE TVLSI (2019-present)
- Associate Editor of IEEE Access (2019-present)
- Associate Editor of IET EL (2020-present)
- Editor of IJCTA (2020-present)
- Guest Editor of IEEE TCAS-II (ISCAS'2021, ISICAS'2021)
- Vice Chair (2019-2021) and Chair (2021-2023) of IEEE Macau CAS Chapter
- Technical Committee of IEEE CASCOM (2020-present)
- Review Committee Member of ISCAS'2021
- TPC Co-Chair of ICCS'2021
- Tutorial Chair of ICCS'2020
- Advisory Committee of APCCAS'2021
- Local Organization Committee of A-SSCC'2019
- Track Chair of A-SSCC'2021, ICTA'2021, ISCAS'2021, APCCAS'2020, APCCAS'2019
- TPC of A-SSCC'2021-present
- TPC of ICECS'2021-present
- TPC of APCCAS'2019-present
- TPC of NorCAS'2020-present
- TPC of ICTA'2020-present
- TPC of ICSICT'2020

AWARDS

- Macao Science and Technology Invention Award'20 (First Prize)
- Best Student Paper Award (Third Place) in the IEEE Radio Frequency Integrated Circuits (RFIC 2021) Symposium
- Top five Associate Editors of IEEE Transaction on Very Large Scale Integration (TVLSI) Systems in 2020
- Best Paper Award in the IEEE Asia Pacific Conference on Circuits and Systems (APCCAS 2019)
- "Haixi" (three places across the Straits) postgraduate integrated circuit design competition (Second Prize) in 2009

CURRENT GROUP MEMBERS

Ph.D. student
Yunbo Huang, 2018
Lin Wang, 2019
Chaowei Yang, 2020
Kai Cheng, 2020
Yue Wu, 2021

M.Sc.
Mei Han, 2019
Gao Zhang, 2020
Bofu Su, 2020
Xionghui Zhou, 2021

POST-DOC./R.A.
Xiaoteng Zhao, 2017
Hao Guo, 2017

SELECTED PUBLICATIONS

- X. Zhao, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.0285-mm² 0.68-pJ/bit single-loop full-rate bang-bang CDR without reference and separate FD pulling off an 8.2(Gb/s)/μs acquisition speed of PAM-4 input in 28-nm CMOS," IEEE Journal of Solid-State Circuits (JSSC), vol. xx, no. xx, pp. xxxx-xxxx, xxx. 2021. [In press]

- H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 5.0-to-6.36GHz wideband-harmonic-shaping VCO achieving 196.9dBc/Hz peak FOM and 90-to-180kHz 1/f³ PN corner without harmonic tuning," IEEE International Solid-State Circuits Conference (ISSCC), pp. 294-296, Feb. 2021.

- H. Guo, Y. Chen, P.-I. Mak, and R. P. Martins, "A 0.08 mm² 25.5-to-29.9GHz multi-resonant-RLCM-tank VCO using a single-turn multi-tap inductor and CM-only capacitors achieving 191.6-dBc/Hz FOM and 130kHz 1/f³ PN corner," IEEE International Solid-State Circuits Conference (ISSCC), pp. 410-412, Feb. 2019.

- Z. Yang, Y. Chen, S. Yang, P.-I. Mak, and R. P. Martins, "A 25.4-to-29.5GHz 10.2mW isolated-sub-sampling PLL (iSS-PLL) achieving -252.9dB jitter-power FOM and -63 dBc reference spur," IEEE International Solid-State Circuits Conference (ISSCC), pp. 270- 272, Feb. 2019.

- Y. Chen, P.-I. Mak, H. Yu, C. C. Boon, and R. P. Martins, "An area-efficient and tunable band width-extension technique for a wideband CMOS amplifier handling 50+ Gb/s signaling," IEEE Transactions on Microwave Theory and Techniques (TMTT), vol. 65, no. 12, pp. 4960-4975, Dec. 2017.

Ka-Fai Un (Keith)
Assistant Professor, IEEE Member
Secretary, Pedagogic Committee,
Institute of Microelectronics
Member, Microelectronics Education Committee,
Institute of Microelectronics

Room 3006, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4450 | Email: kafaiun@um.edu.mo

RESEARCH INTERESTS

Wideband analog transmitter
MIMO transmitter
Digital transmitter
Multi-phase local oscillator generation
Digital phase-locked loop
Switched-capacitor circuit
Ultra-low power analog neural network-based classifier
In-memory-computation for artificial intelligence
Convolutional neural network digital accelerator

PROFESSIONAL SERVICES

- Secretary of IEEE CASS Macau Chapter
- Reviewer of IEEE JSSC, T-CAS I/II, Access, ISCAS, etc

AWARDS

- IEEE (Macau Chapter) Project Competition Champion'21 (co-supervisor)
- Synopsys Microelectronics Award'14
- PhD student recipient of Postgraduate Science and Technology Research and Development Award'12
- Merit Student Paper in Asia Pacific Conference on Circuits and Systems'08
- Presidential award, National Taiwan University'04
- Macau Representative for International Mathematics Olympiad'03
- Macau Representative for Chinese Mathematics Olympiad'03

CURRENT GROUP MEMBERS

Ph.D.
Yuzhao Fu, 2020
Jixuan Li, 2019
Feifei Chen, 2018 (co-supervisor)
Ran Zhang, 2019 (co-supervisor)

M.Sc.
Jinhai Lin, 2020
Jiabao, Chen, 2020
Lei Xuan, 2019 (co-supervisor)

SELECTED PUBLICATIONS

- K. -F. Un, F. Zhang, P. -I. Mak, R. P. Martins, A. Zhu and R. Staszewski, "Design Considerations of the Interpolative Digital Transmitter for Quantization Noise and Replicas Rejection," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 1, pp. 37-41, Jan. 2020.
- K. -F. Un, G. Qi, J. Yin,; S. Yang, S. Yu, C.-I. Ieong, P.-I. Mak, R. P. Martins, "A 0.12-mm² 1.2-to-2.4-mW 1.3-to-2.65-GHz Fractional-N Bang-Bang Digital PLL With 8-µs Settling Time for Multi-ISM-Band ULP Radios," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 66, no. 9, pp. 3307-3316, Sept. 2019
- W. Yu, K. Un, P. Mak and R. P. Martins, "A 0.7–2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 14-25, Jan. 2018.
- K. Un, W. Yu, C. Cheang, G. Qi, P. Mak and R. P. Martins, "A Sub-GHz Wireless Transmitter Utilizing a Multi-Class-Linearized PA and Time-Domain Wideband-Auto I/Q-LOFT Calibration for IEEE 802.11af WLAN," IEEE Transactions on Microwave Theory and Techniques, vol. 63, no. 10, pp. 3228-3241, Oct. 2015.
- K.-F. Un, P.-I. Mak, and R. P. Martins, "A 53-to75-mW, 59.3-dB HRR, TV-Band White-Space Transmitter using a Low-Frequency Reference LO in 65-nm CMOS," IEEE Journal of Solid-State Circuits, vol. 48, no.8, pp. 2078-2089, Sep. 2013.

Mo Huang
Assistant Professor, IEEE Senior Member
Member, Industrial Collaboration and Microelectronics Center/ZUMRI, Institute of Microelectronics

Room 3014, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-8036 | Email: mohuang@um.edu.mo

RESEARCH INTERESTS

DC-DC Converters
GaN Drivers
Wireless power transfer and energy harvesting
Analog and mixed-signal IC design

PROFESSIONAL SERVICES

- Associate Editor, Microelectronic Journals, 2021
- TPC Member, IEEE VLSI-DAT, 2021
- TPC Member, IEEE ICESC, 2020
- TPC Member, APCCAS 2018
- TPC Member, ICTA 2017, 2021
- TPC Member, ASICON 2017
- Reviewer of IEEE JSSC, TPE, TCAS-I, TCAS-II, TVLSI, EL, etc.

AWARDS

- IEEE ISSCC Takuo Sugano Award'17
- IEEE TENCON Professional Award'15

CURRENT GROUP MEMBERS

Ph.D.
Tingxu Hu, 2020
Qiujin Chen, 2020

M.Sc.
Yunzhe Yang, 2020
Zihan Yang, 2020

POST-DOC./R.A.
Jian Liu, 2020
Jinxu Xu, 2020
Yuanfei Wang, 2021

SELECTED PUBLICATIONS

- M. Huang, Y. Lu, T. Hu, and R. P. Martins, "A Hybrid Boost Converter With Cross-Connected Flying Capacitors," IEEE Journal of Solid-State Circuits (JSSC), vol. 56, no. 7, pp. 2102–2112, Jul. 2021. [Also in ISSCC 2020].
- T. Hu, M. Huang, Y. Lu, X. Y. Zhang, F. Maloberti, and R. P. Martins, "A 2.4-GHz CMOS Differential Class-DE Rectifier with Coupled Inductors," IEEE Transactions on Power Electronics (TPE), access for publication .
- M. Huang, Y. Lu, and R. P. Martins, "An Analog-Proportional Digital-Integral Multiloop Digital LDO With PSR Improvement and LCO Reduction," IEEE Journal of Solid-State Circuits (JSSC), vol. 55, no. 6, pp. 1637–1650, Jun. 2020 [Also in CICC 2019].
- M. Huang et al., "Single- and Dual-Band RF Rectifiers with Extended Input Power Range Using Automatic Impedance Transforming," IEEE Transactions on Microwave Theory and Techniques (TMTT), vol. 67, no. 5, pp. 1974–1984, May 2019.
- M. Huang, Y. Lu, S. U, and R. P. Martins, "An Analog-Assisted Tri-Loop Digital Low-Dropout Regulator," IEEE Journal of Solid-State Circuits (JSSC), vol. 53, no. 1, pp. 20–34, Jan. 2018 [Also in ISSCC 2017].
- M. Huang, Y. Lu, and R. P. Martins, "A Reconfigurable Bidirectional Wireless Power Transceiver for Battery-to-Battery Wireless Charging," IEEE Transactions on Power Electronics (TPE), vol. 34, no. 8, pp. 7745–7753, Aug. 2019 [Also in ISSCC 2017].

Ka-Meng Lei
Assistant Professor, IEEE Member
Member, Lab Infrastructure and Testing Facilities Committee, Institute of Microelectronics

Room 3015f, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4432 | Email: kamenglei@um.edu.mo

EDUCATION

PhD, ECE, University of Macau, 2016
BS, EEE, University of Macau, 2012

EXPERIENCES

- Assistant Professor, University of Macau, Macau, Sept. 2019 - present
- Visiting scholar, Harvard University, Cambridge, MA, Jun. 2017 – Aug. 2019
- Lecturer (UM Macao Fellow), University of Macau, Macau, Dec. 2016 – Aug. 2019
- Research assistant, University of Macau, Macau, Sept. 2012 – Nov. 2016
- Trainee, Evatronix SA, Poland, Jun. 2012 – Jul. 2012

RESEARCH INTERESTS

Analog and RF circuit techniques for micro-NMR
Sensors and analog front-end interfaces
System planning and integration for biomedical devices
Ultra-low-power and ultra-low-voltage IC design

PROFESSIONAL SERVICES

- Demo Session Chair, IEEE ICECS 2019
- Organizing Committee, IEEE A-SSCC 2019
- YP Committee member, IEEE SSCS, 2020 – present
- TPC Member, IEEE ICTA 2021

AWARDS

- IEEE Solid-State Circuits Society - Pre-Doctoral Achievement Award 2017
- FDCT Macao Science and Technology Award for Postgraduates2016 (Ph.D. level)
- IEEE international Solid-State Circuits Conference - Silkroad Award 2016
- IEEE Asian Solid-State Circuits Conference - Distinguished Design Award 2015
- Chemical and Biological Microsystems Society - Student/Young Researcher Grant 2015
- Asia Symposium on Quality Electronic Design – Best Paper Award 2013

CURRENT GROUP MEMBERS

Ph.D.
Liwen Lin, 2019 (co-supervisor)
Shuhao Fan, 2019
Rui Luo, 2020
Qi Zhou, 2020
Dan Shi, 2021
Haihua Li, 2021

M.Sc.
Kanghong Yu, 2020
Hengchen Zou, 2020
Chengyu Che, 2021

SELECTED PUBLICATIONS

- K.-M. Lei, P.-I. Mak, and R. P. Martins, "A 0.35-V 5,200-µm2 2.1-MHz Temperature-Resilient Relaxation Oscillator with 667fJ/cycle Energy Efficiency Using an Asymmetric Swing-Boosted RC Network and a Dual-Path Comparator," IEEE J. Solid-State Circuits, Early access, 2021.
- K.-M. Lei, P.-I. Mak, and R. P. Martins, "Startup time and energy-reduction techniques for crystal oscillators in the IoT era," IEEE Transactions on Circuits and System II - Express Briefs, vol. 68, no. 1, pp. 30-35, Jan. 2021.
- K.-M. Lei, D. Ha, Y.-Q. Song, R. M. Westervelt, R. P. Martins, P.-I. Mak, and D. Ham, "Portable NMR with parallelism," Analytical Chemistry, vol. 92, no. 2, pp. 2112-2120, Jan. 2020.
- A. Dupré*, K.-M. Lei*, P.-I. Mak, R. P. Martins, and W. K. Peng, "Micro- and nanofabrication NMR technologies for point-of-care medical applications – A review," Microelectronic Engineering, vol. 209, pp. 66-74, Mar. 2019.
- K.-M. Lei, P.-I. Mak, M.-K. Law, and R. P. Martins, "A regulation-free sub-0.5-V 16-/24-MHz crystal oscillator with 14.2-nJ startup energy and 31.8-µW steady-state power," IEEE J. Solid-State Circuits, vol. 53, no. 9, pp. 2624-2635, Sept. 2018 [Also in ISSCC 2018].
- K.-M. Lei, H. Heidari, P.-I. Mak, M.-K. Law, F. Maloberti and R. P. Martins, "A Handheld High-Sensitivity Micro-NMR CMOS Platform with B-Field Stabilization for Multi-Type Biological/Chemical Assays," IEEE Journal of Solid-State Circuits, vol. 52, Jan. 2017. [Also in ISSCC 2016]

Minglei Zhang
Assistant Professor
IEEE Member

Room 4023, 4/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-4445 | Email: mlzhang@um.edu.mo

RESEARCH INTERESTS

High-Speed ADCs
Hybrid ADCs
ADC-based Optical Receiver
Mixed-Signal Computing
Time-Domain Integrated Circuits

PROFESSIONAL SERVICES

- Reviewer of IEEE JSSC, SSCL, TCAS-I, TCAS-II, TVLSI, TPE, Sensor Journal, Access, etc.

CURRENT GROUP MEMBERS

Ph.D.
Zehang Wu, 2020 (co-supervisor)

M.Sc.
Chaorui Zou, 2020 (co-supervisor)

SELECTED PUBLICATIONS

- M. Zhang, Y. Zhu, C. H. Chan, and R. P. Martins, "A 8-bit 10-GS/s 16× interpolation-based time-domain ADC with <1.5-ps uncalibrated quantization steps," IEEE Journal of Solid-State Circuits, vol. 55, no. 12, pp. 3225-3235, Dec. 2020.

- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 0.6-V 13-bit 20-MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed enhanced techniques," IEEE Journal of Solid-State Circuits, vol. 54, no. 12, pp. 3396-3408, Dec. 2019.

- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 4× interleaved 10GS/s 8b time-domain ADC with 16× interpolation-based inter-stage gain achieving >37.5dB SNDR at 18GHz input," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2020, pp. 252-253.

- M. Zhang, C. H. Chan, Y. Zhu, and R. P. Martins, "A 0.6V 13b 20MS/s two-step TDC-assisted SAR ADC with PVT tracking and speed enhanced techniques," IEEE International Solid-State Circuits Conference (ISSCC), Feb. 2019, pp. 66-67.

Yang Jiang (Tim)
Assistant Professor
IEEE Member

Room 4027, 4/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-9939 | Email: timjiang@um.edu.mo

RESEARCH INTERESTS

- Integrated Power Converters
- Power/Sensor Device Drivers
- Power Management for Energy Harvesting

PROFESSIONAL SERVICES

- Member of Power and Energy Circuits and Systems Technical Committee (PECAS), IEEE CASS
- TPC and RC Member of IEEE ICECS, 2020
- Review Committee Member of IEEE APCCAS, 2019
- Peer Reviewer of:
  - IEEE Journal of Solid State Circuits (JSSC)
  - IEEE Solid-State Circuits Letters (SSC-L)
  - IEEE Transactions on Circuits and Systems I: Regular Papers (TCAS-I)
  - IEEE Transactions on Circuits and Systems II: Express Briefs (TCAS-II)
  - IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)
  - IEEE Access
  - Microelectronics Journal
  - IEICE Electronics Express
  - IEEE ISCAS, ICECS, APCCAS, BioCAS, ASQED…

AWARDS

- IEEE Solid-State Circuits Society Pre-Doctoral Achievement Award 2018-2019
- Macau FDCT Scientific and Technological R&D Award for Postgraduates, 2020 (Ph.D. class)

CURRENT GROUP MEMBERS

Ph.D.
Feiyu Li, 2021
Guangshu Zhao, 2019 (co-supervisor)

M.Phil./M.Sc.
Qiaobo Ma, 2020
Xiongjie Zhang, 2020
Ruijie Zhao, 2020
Huihua Li, 2021
Xuchu Mu, 2021

SELECTED PUBLICATIONS

- Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algebraic Series-Parallel-Based Switched-Capacitor DC-DC Boost Converter with Wide Input Voltage Range and Enhanced Power Density," IEEE J. Solid-State Circuits (JSSC), vol. 54, no. 11, pp. 3118-3134, Nov. 2019.

- Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "Algorithmic Voltage-Feed-In Topology for Fully Integrated Fine-Grained Rational Buck-Boost Switched-Capacitor DC-DC Converters," IEEE J. Solid-State Circuits (JSSC), vol. 53, no. 12, pp. 3455-3469, Dec. 2018. [Also in ISSCC'18]

- J. Wu, K.-C. Lei, H.-M. Leong, Y. Jiang*, M.-K. Law, P.-I. Mak, and R. P. Martins, "Fully Integrated High Voltage Pulse Driver Using Switched-Capacitor Voltage Multiplier and Synchronous Charge Compensation in 65-nm CMOS," IEEE Trans. Circuits Syst. II Exp. Briefs, vol. 66, no. 10, pp. 1768-1772, Oct. 2019. (*Corresponding Author)

- J. Wu, H. -M. Leong, Y. Jiang*, M. -K. Law, P. -I. Mak and R. P. Martins, "A Fully Integrated 10-V Pulse Driver Using Multiband Pulse-Frequency Modulation in 65-nm CMOS," IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 29, no. 9, pp. 1665-1669, Sept. 2021. (*Corresponding Author)

- Y. Jiang, M. K. Law, P. I. Mak and R. P. Martins, "An Arithmetic Progression Switched-Capacitor DC-DC Converter with Soft VCR Transitions Achieving 93.7% Peak Efficiency and 400 mA Output Current," in IEEE Asian Solid-State Circuits Conference (A-SSCC), Nov. 2021.

Wei-Han Yu (Hank)
Assistant Professor, IEEE Member
Member, Lab Infrastructure and Testing Facilities Committee, Institute of Microelectronics

Room 3006, 3/F, N21, University of Macau, Taipa, Macau, China
Tel.: +853-8822-8792 | Email: hankyu@um.edu.mo

RESEARCH INTERESTS

Low-power IoT transceivers
Machine learning analog / digital accelerators
In-memory processing
Circuits for AI
MIMO wireless transceivers
Energy harvesting
Artificial retina
Switched-capacitor circuits
FPGA for AI

PROFESSIONAL SERVICES

- Committee of IEEE SSCS Young Professional
- Reviewer of IEEE JSSC, T-CAS I/II, ISCAS, etc

AWARDS

- IEEE (Macau Chapter) Project Competition Champion'21, supervisor
- IEEE Young Professionals Hall of Fame Award'20
- IEEE ISSCC SRP Poster Award (Honorable Mention)'19, co-author
- IEEE SSCS Pre-doctoral Achievement Award'18
- Synopsys Academic Prize, Synopsys (Macau)'18
- Macau Talent Award'18
- FDCT S&T Postgraduate Student Award'16
- IEEE ISSCC STGA Award'16
- CEM, ChipIdea and Ocean-Tech Prize'10
- Choi Kai Yau Scholarship'07
- FST Dean's Honor List, University of Macau'07

SELECTED PUBLICATIONS

- W.-H. Yu, H. Yi, P.-I. Mak, J. Yin, R. P. Martins, "A 0.18V 382µW Bluetooth Low-Energy (BLE) Receiver with 1.33nW Sleep Power for Energy-Harvesting Applications in 28nm CMOS," IEEE International Solid-State Circuits Conference (ISSCC), Digest., pp. 414-415, Feb. 2017. [Chip Olympics] [ISSCC 2017 Technical Highlight]

- W.-H. Yu, M. Giordano, R. Doshi, M. Zhang, P.-I. Mak, R. P. Martins, and B. Murmann, "A 4-bit Mixed-Signal MAC Array with Swing Enhancement and Local Kernel Memory," IEEE International Midwest Symposium on Circuits and Systems, Aug. 2021.

- W.-H. Yu, K.-F. Un, P.-I. Mak and R. P. Martins, "A 0.7–2.5 GHz, 61% EIRP System Efficiency, Four-Element MIMO TX System Exploiting Integrated Power-Relaxed Power Amplifiers and an Analog Spatial De-Interleaver," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 65, no. 1, pp. 14-25, Jan. 2018.

- Chao Fan, Wei-Han Yu, Pui-In Mak, R. P. Martins, "A 40-Gb/s PAM-4 Transmitter Using a 0.16-pJ/bit SST-CML-Hybrid (SCH) Output Driver and a Hybrid-Path 3-Tap FFE Scheme in 28-nm CMOS," IEEE Transactions on Circuits and Systems I, vol. 66, pp. 4850–4861, Dec. 2019.

SKL-AMSV Innovation Centers

Wireless and Multidisciplinary Innovation Center (WMIC)

To develop circuit techniques devoted to practical problems, to invent new concept-to-solution designs to underpin the development of wireless industry, and to develop advanced micro/hybrid systems that can be applicable to human beings, with research in biology and chemistry. Several key directions are highlighted:

- Ultra-low-power ZigBee and Bluetooth Low Energy (BLE) radios for low-power low-cost wireless connectivity such as Internet of Things.
- Wideband flexible receivers and transmitters for 5G communications.
- Micro-power analog circuits with enhanced performances, power and area efficiencies.
- Electronics-automated digital microfluidics with software-defined intelligence.
- Portable nuclear magnetic resonance (NMR) electronics for precision medicine.
- Ultra-low-power solar-powered CMOS/beyond-CMOS sensing chips.

Wireless IC

This research line focuses on RF and mmWave ICs for a wide variety of applications, including but not limited to, 3G/4G/5G multi-standard cellular radios, ultra-low-cost ultra-low-power IoT radios, and tens-of-MHz radios for micro-nuclear magnetic resonance (μNMR) applications. The key research interests are:

- Sub-6GHz 2G/3G/4G wireless transceiver front-ends, and >28GHz 5G transceiver front-ends. SAW-less RF-flexible receivers and transmitters using our proposed gain-boosted N-path filter techniques are investigated.
- Ultra-low-power IoT transceiver front-ends from sub-GHz to 2.4GHz, conforming to Bluetooth Low Energy (BLE), ZigBee and NB-IoT. Ultra-low-cost and ultra-low-power RF and baseband (BB) techniques using our proposed function-reuse gain-boosted N-path receiver, RF-to-BB-current-reuse receiver, function-reuse VCO-PA, and ultra-low-voltage receiver, transmitter and frequency synthesizer using a local micro-power manager are investigated.
- Analog baseband circuits such as micro-power amplifiers with high capacitive load drivability, continuous-time/discrete-time filters with a very compact chip area, energy-harvesting units with high efficiency, sensor readout interfaces with low noise effective factor, and crystal oscillators with low startup energy are investigated.
- RF/mmWave circuits such as active-inductor-enhanced wideband amplifiers, multi-harmonic-peaking wave-shaping VCOs, time-interleaved ring oscillators with a wide tuning range, and type-I phased-locked loops with ultra-low-voltage operation are investigated.
- Digital baseband correction techniques for I/Q mismatch, LO feedthrough and strong-memory-effect distortion in wideband transmitters are investigated.
- Tens-of-MHZ (e.g., 20MHz) transceivers with a sensing coil (on/off-chip spiral inductor) to allow electronic-automated biological and chemical assays in a small form factor.

The invented techniques are expected to advance the state-of-the-art knowledge in the fields, and should be potentially transferrable to the industry for practical applications.

Biomedical IC

The research line focuses on advanced micro/hybrid systems that can be applicable to human beings, biological and chemistry researches. The key research interests are:

- Advanced electronics platform for small animal behavioral study. Miniaturized circuit/SoC for simultaneous extracellular electrophysiology recording and optogenetic neural manipulation is studied.

- Micro ultrasound transducer for biological imaging and measurement. New membrane structure CMUT is designed and fabricated based on MEMS technology to enhance the output ultrasonic pressure. Multi-frequency CMUT is investigated to extend the imaging capability of photoacoustic imaging.

- Intra-body Communication with study in physical layer and MAC layer and their IC implementation.

- Microprocessor with built in multi-tasking ability for biomedical engineering applications. This can be used as a platform for ASIC development for related applications.

- Ultra-low-power energy harvesting CMOS biomedical implantable sensing chip. Single-chip energy harvesting solution with various ambient sources for low voltage operation, high efficiency and ultra-compact form factor are investigated.

- Ultra-low power biopotential interfacing circuit. Nanowatt analog signal processing and filtering is studied, focusing on nanowatt circuit design, subthreshold operation, linearity improvement and gain compensation.

- Digital microfluidic chips with software-defined intelligence. On-chip 3D structures for precise droplet splitting, fuzzy-logic and real-time feedback for precise droplet positioning, and non-DC driving voltage wave- forms for higher droplet moving speed are investigated.

  The invented techniques are expected to advance the state-of-the-art in terms of performances and understanding, and should be transferrable to the industry for practical applications.

Data and Power Conversion Innovation Center (DPIC)

The main objective of this center is to focus on innovative research and development of high-performance data conversion and signal processing analog front-ends ICs and integrated power ICs including:

- Analog-to-Digital Converters (ADCs)
- Video/ Audio Codecs
- Power converters
- Data conversion interface for wireless and wireline communication
- Signal processing analog frontends for sensors and autonomous systems
- High efficiency, wide input range, wide load current range, and fast response power management DC-DC converters, low dropout regulators, etc.

Data Conversion and Signal Processing

The main objective of the research line is focus on innovations on high-performance data conversion and signal processing analog ICs, including those covering the most emerging applications e.g. 4G LTE, LTE-A, Ultra Low Power IoT devices, wideband (wirelined- or optical communication), etc. The following lists the key research interests:

- Power efficient data converters for portable and autonomous IoT system. The projects are based on the dynamic based circuits, like inverters, comparators, successive approximation register (SAR), binary search ADC etc. to achieve very low power consumption data converter implementation.

- Digitally-assisted / calibrated high resolution CMOS data converters for high quality video, cellular and data acquisition front-ends. This projects study the innovation that relies on the advanced scaling nanometer CMOS technology that bring the strong processing power of digital circuits, to assist the detection and calibration of the various analog circuit non-idealities like offset/gain errors, nonlinearity, various mismatch among different channels, etc.

- Oversampling noise-shaped sigma-delta converter for wireless applications. This project concentrates on the innovation techniques improving the noise-shaping performance in the discrete-time and continuous-time sigma-modulator modulator.

- Ultra wide bandwidth data converters for optical communications. This project investigates different techniques to extend the bandwidth physical limits in the data converter. The possible direction includes the interleaving with calibration or compensation of various mismatches, and utilize the time-based converters to take advantages of technology scaling.

- Application of data converters in various electronics application including sensors, power converters and navigation systems. This project focused more on the application aspect of the data converters. Current projects include the design of sensing interface for power electronics converters, and an accelerometer/ velocity meter/position meter sensing analog sigma-delta front-end interface for navigation systems.

Integrated Power

The research directions are:

- Integrated power electronics controller design: The integrated power electronics controller can significantly improve the power electronics system performances and is easy to be implemented by others (without knowledge and save programming time) compared with conventional DSP controller. Moreover, the integrated power electronics controller is possible to replace the digital controller in the power compensator products. This research work focuses on programmable gain signal conditioning circuit, analog-to-digital (A/D) conversion, and pulse-width-modulation (PWM) generator. Up to now, there is no such three-phase power electronics controller IC in the market.

- Power management IC design: Fully-integrated high efficiency, wide input range, wide load current range, small output ripple, and fast transient response power management circuits, including inductor-based and switched-capacitor DC-DC converters, low dropout regulators, etc. are of great interest.

- Wireless power transfer: Wireless power transfer (WPT) has a wide range of applications including (arranged from low to high power levels) radio frequency identification (RFID), internet-of-things (IoT), implantable medical devices (IMDs), real-time wireless power for non-contact memory devices and wafer-level testing, and also wireless chargers for portable/wearable devices and electric vehicles (EVs). It is evident that the utilization of WPT technologies is on the critical point of exponential growth.

The research line aimed at the investigation of the advantages of using microelectronics through signal processing and intelligence in order to improve the performance of energy processing power electronics systems, which is related with software control and hardware IC implementation. Power management and wireless power transfer are our research focuses.

SKL-AMSV Innovation Centers

Microelectronics Research Center at Zhuhai UM S&T Research Institute (SKL-AMSV Hengqin Branch)

模拟与混合信号超大规模集成电路
国家重点实验室（横琴分部）

State Key Laboratory of
Analog and Mixed-Signal VLSI
(Hengqin Branch)

In response to the Development Plan Outlines for the Guangdong-Hong Kong-Macao Greater Bay Area, the Microelectronics Research Center (MRC) at Zhuhai UM S&T Research Institute (ZUMRI) was established in 2019, aiming at demonstrating a successful example of research technology commercialization in Zhuhai Hengqin, connecting Macau with the other cities in the Greater Bay Area. The Microelectronics Research Center operates as a Hengqin Branch of the State Key Laboratory of Analog and Mixed-Signal VLSI of the University of Macau (UM), providing one more platform and opportunity for UM microelectronics professors to conduct applied research and development. Also, Hengqin has a much larger area compared to Macau, attracting UM graduates to stay and helping UM professors to expand their research groups. With such, the Institute of Microelectronics at UM greatly boosts the number of graduate students, nurturing more skilled and talented engineers not only for Macau and Hengqin, but also for the whole IC industry of China.

The satellite Hengqin Branch serves as the following functions:

- Absorbing government funds and commercial projects in Mainland China.
- Providing more lab and office spaces for more UM graduate students.
- Recruiting post-doctoral researchers and research assistants for UM professors.
- Incubating startup companies of UM microelectronics professors.
- Organizing academic-industrial cooperation forums and technical workshops.
- Setting up an open integrated circuit testing laboratory for the region.

In 2020, UM professors attracted over 10 million CNY research funds, mostly from the industry, through the MRC at ZUMRI. As of Oct. 2021, there are about 10 UM professors undertaking more than 20 projects funded by the National Natural Science Foundation of China (NSFC), the Ministry of Science and Technology of China, Guangdong Province, Zhuhai City, and several Top China IC design companies. Currently, there are 3 post-doctoral researchers and 8 research assistants working in the “Phase-I” space, while the “Phase-II” space is expected to start operating with more manpower in early 2022.

In addition, the MRC helped UM and ZUMRI on co-organizing several influential technical forums and workshops in Mainland, including but not limited to the Workshop on IC Advances in China (ICAC), ISSCC China promotion and press conferences, considerably increased the reputation of UM and the SKL-AMSV in the Greater Bay Area and beyond.

THESES AWARDED

Ph.D. (31)

Chao FAN
Power-Efficient Ultra-High-Speed Communication Circuit Techniques in Nanoscale CMOS, 2020 Lecturer, Xi'an Jiaotong University

Mingqiang GUO
Mismatch Calibration Techniques for Low-Power High-Speed Time-Interleaved ADC, 2020 UM Macao
Post-Doctoral Fellowship (UMPF), University of Macau

Wenning JIANG
High Performance Gigahertz Nyquist ADC Designs, 2020 Post-Doctoral Fellow, University of Macau

Mingzhong LI
Patterned Surface Wettability and Advanced Droplet Manipulation Techniques for Disease Diagnostics using Digital Microfluidics, 2020
Post-Doctoral Fellow, University of Macau

Xiaofei LI
Design of Radio Frequency Wireless Power Transfer Circuits, 2020
Post-Doctoral Fellow, Zhuhai UM Science & Technology Research Institute

Jie LIN
Single Stage Regulating Rectifiers for Wireless Power Transfer, 2020
Senior Engineer, Hisilicon

Fangyu MAO
Design and Analysis of Near-Field Wireless Power Transfer Circuits and Systems, 2020
UM Macao Post-Doctoral Fellowship (UMPF), University of Macau

Panke WANG
A Real-time Neural Spike Sorting System and Its Application on Neural Decoding, 2020
Assistant Professor, Guangzhou University of Chinese Medicine

Wen-Liang ZENG
Design, Control and Analysis of Integrated DC-DC Converters for Low Power Applications, 2020
Post-Doctoral Fellow, Microelectronics Research Center of the Zhuhai UM Science & Technology Research Institute

Liang QI
Low-Power Cascaded Delta-Sigma Modulator for Wideband Telecommunication Applications, 2019
Assistant Professor, Shanghai Jiaotung University

Wei WANG
Design of Low-Power Mega to Hundred Mega Hz Bandwidth CTDSM, 2019
Engineer, Hisilicon

Biao WANG
Resolution Enhancement Techniques for Multi-Bit Incremental ADC, 2019
Engineer, Hisilicon

Shiheng YANG
Power-Efficient Analog and Digital Frequency Synthesizers in Nanoscale CMOS, 2019
Professor, University of Electronic Science and Technology of China

Xiaofeng YANG
Low power and low phase noise phase-locked loop, oscillators and clock receiver design, 2019
CFO, Reexen Technology Co.,Ltd

Haidong YI
Ultra-Low-Voltage Analog and RF Circuit Techniques for Short-Range Wireless Radios in Nanoscale CMOS, 2019
Engineer, Hisilicon/Huawei

Shuang ZHANG
Galvanic Coupling Human Body Communiction Channel Modeling for Medical Implantable Devices Communication (MIDC), 2019
Lecturer, Neijing Normal University

Da FENG
Polyphase Decomposition for Sigma-Delta A/D Converters, 2018
Civil Servant, Macau

Yang JIANG
Design of Fully Integrated Fined-Grained Switched-Capacitor DC-DC Topologies in Bulk CMOS, 2018
Assistant Professor, University of Macau

Jianwei LIU
Design Techniques for Energy Efficient ADCs, 2018
Senior Design Engineer, United Microelectronics Center, Chongqing, China

Xingqiang PENG
Ultra-Low-Power Wireless Transmitter Circuit Techniques for Internet-of-Things Applications, 2018
Engineer, Hisilicon/Huawei

Jiujia WANG
Practical Modeling of Membrane Deflection for Collapse Mode CMUT through Model Verification, 2018
Research Assistant Professor, University of Macau

Dezhi XING
Advanced Techniques in Analog to Digital Converters, 2018
Senior Analog Design Engineer, Chongqing Jixin Microelectronics Tech Co. Chongqing, China

THESES AWARDED

Ph.D. (31) (CONTINUED)

Tantan ZHANG
Nano-Watt Class CMOS Interface Circuits for Wireless Sensor Nodes, 2018
Research Scientist, A*Star Singapore

Chak-Fong CHEANG
Digital Correction Techniques for I/Q Mismatch, LO Feedthrough and Distortion in Wideband Transmitters, 2017
Engineer, Mediatek

Zhiyuan CHEN
Efficient Power Management Design for Energy Harvesting Biomedical Applications, 2017
Associate Professor, Fudan University

Changhao CHEN
Circuits and Noise modelling for extracellular electrophysiology recording and optogentic neural manipulation, 2017
Post-Doctoral Fellow, Univerisity of Macau

Cheng DONG
Electronic-Automated Digital Microfluidic System for Multi-Analysis, 2017
CFO, DigiFluidic

Arshad Hussain
High-Resolution Passive and Active-Passive Switched-Capacitor Delta-Sigma Modulator Design Techniques in Nanoscale CMOS, 2017
Assistant Professor, Quaid-i-Azam University, Pakistan

Gengzhen QI
SAW-Less Multiband TDD/FDD Transceiver Front-Ends Using Gain-Boosted N-path Techniques, 2017
Associate Professor, Sun Yat-Sen University

Wei-Han YU
Power-Efficient and Wideband WLAN Transmitter Techniques in Nanoscale CMOS, 2017
Lecturer/Macau Fellow, University of Macau

Yuanyu YU
Design and Characterization of Embossed Membrane CMUTs for Improving Output Pressure, 2017
Post-Doctoral Fellow, Univerisity of Macau

M.Sc. (37)

Chi-Wa CHAO
Study and Design of Quasi-Proportional-Resonant Controllers for Grid-Connected Inverter, 2020
Assistant Engineer, New Vector Engineering Design & Consultancy Co. Ltd. Macau, China

Shaocan FAN
Effective Heart Sound Segmentation Using Deep Neural Networks for Valvular Heart Disease Diagnosis, 2020
Ph.D. Student, Sun Yat Sen University

Haoyu GONG
Oversampling Data Converter with LDO-free Power Management System, 2020
Ph.D. student, University of Macau

Ka-Chon LEI
Fully Integrated High Voltage Pulse Driver Using Switched-Capacitor Voltage Multiplier and Synchronous Charge Compensation in 65nm CMOS, 2020
Engineer, AkroStar

Hou-Man LEONG
Fully Integrated High Voltage Pulse Driver with Multi-band Pulse-Frequency Modulation in 65nm CMOS, 2020
Engineer, AkroStar

Kejin LI
Low Power ECG SAR ADC Design and Consideration, 2020
Research Assistant, ZUMRI

Hanyu WANG
LDO-Free Power Management System for Energy-Harvesting Data Acquisition Applications, 2020
Analog Design Engineer, AMicro Co., Zhuhai, China

Chuanqi WEI
Low Complexity Template-Model-Based Motion Vector Motion Detection for CMOS Image Sensor, 2020
Engineer, Cambrian

Tai ZHANG
A Switched-Capacitor DC-DC Converter with Adaptive Single-Boundary Hysteretic Control, 2020
Engineer, Thinkplus Semiconductor, Shenzhen

Jianyang DENG
Instantaneous Power Quality Indices Detection Under Frequency Deviated Environment, 2019
IT Technical Specialist, Macau CTM, Macau, China

Xinyi GE
Analysis of Jitter in Bang-Bang Clock and Data Recovery Circuit, 2019
Engineer, Qualcomm (Shanghai) Ltd.

Yibo HAN
An automatic multi-channel cell impedance-based measurement system for real-time cell feature monitoring, 2019

Xuewei LEI
Low Power and Low Resolution Phase Domain ADC Design for FSK/PSK Demodulation, 2019
Engineer, Shanghai Awinic Technology Co.,Ltd

Jixuan LI
Design of Battery Management System for Fast and Safe Charging, 2019
Ph.D. student, University of Macau

THESES AWARDED

M.Sc. (37) (CONTINUED)

Junhao LIANG
On the study of Programmable Continuous Time Sigma Delta Modulator for Implantable ECG Acquisition Circuit Application, 2019
Analog Design Engineer, AMicro Co., Zhuhai, China

Ziyang LIN
Design of KY Converter with Constant ON-Time Control under DCM Operation, 2019
Data Analyst, Kong Seng Paging Ltd. Macau, Macau, China

Chi-Lon U
An Approach to Real Time Spike Sorting by using Wavelet Packet Transform and Enhanced Growing Neural Gas, 2019
Engineer, Macau Airport

Yulun WU
A Switched-Capacitor DC DC Converter with Unequal Duty Cycle for Ripple Reduction and Efficiency Improvement, 2019
Engineer, Goodix Technology, Shanghai

Ruping XIAO
Wavelet Transform-Based Ultra-Low Power High Accuracy QRS Detector for Wearable ECG Monitoring Applications, 2019
Engineer, Nvidia

Yukun XU
Curvature Compensated BJT-Based Time-Domain CMOS Temperature Sensor Design, 2019
Engineer, Sino Microelectronics Technology Co. Ltd.

Yi ZHANG
A Computation Resource Friendly Convolutional Neural Network Engine For EEG-based Emotion Recognition, 2019

Lei ZHAO
Design of Digital LDO For Fast Transient Response, 2019
Ph.D. student, Iowa State University, USA

Baoyi CEN
Switched-Capacitor DC-DC Converter with Fixed Output Spectrum Modulation for Noise-Sensitive IoT Applications, 2018
Engineer, China Electric Power Equipment and Technology Co., Ltd.

Zhimin CHEN
Electromagnetic Field Analysis of Low-Magnitude High-Frequency Vibrator with Multiple Plungers, 2018

Yuanqing HUANG
Design and Analysis of Energy Efficieny Analog and Digital LDO Designs, 2018
Ph.D. student, University of Texas at Dallas, USA

Cheng LI
Peripheral Interface CircuitriesAnalysis for High-Speed and -Resolution SAR ADC, 2018
Ph.D. student, University of California, Davis

Jiaji MAO
On the study of Advanced Background Calibration Techniques for High Resolution Split Pipeline Analog to Digital Converter, 2018
Ph.D. student, University of Macau

Dapeng SUN
Process Compensated CMOS Temperature Sensor Exploiting Piecewise Base Recombination Current, 2018
Engineer, Bank of China

Wai-Hong ZHANG
Low-Offset and Low-Noise Comparators with Calibration Techniques, 2018
Engineer, Akrostar Macau

Wenming ZHENG
Analysis, Design and Control of An Integrated Three-Level Buck Converter under DCM Operation, 2018
Senior System Design Engineer, Injoinic Technology, Zhuhai, China

Xutong CUI
Rhythm Sequence based on SVD-entropy for Emotion EEG Signal Analysis, 2017

Xiao JIANG
Reception Performance Enhancement of Capacitive Micromachined Ultrasonic Transducers via Modified Membrane Structures, 2017

Chon-Hei LEI
Design of 0.18μm 10-bit 10MS/s Successive Approximation Analog-to-Digital Converters for Neural Spikes Acquisition, 2017
Engineer, CEM

Xin LIU
Helmholtz Resonant Effect on Air-coupled CMUTs, 2017
Ph.D. student, University of Macau

Ziyang LUO
Design of Ultra Low Power Bandgap Voltage References, 2017
Ph.D. student, University of Texas at Dallas, USA

Yi-Wei TAN
Study, Design and Control of An Integrated 3-Level Boost Converter, 2017
Technical Marketing Engineer, Gree Electric Appliances, Inc. of Zhuhai, Zhuhai, China

Guancheng WANG
Testing signal generation and timing interleaving calibraiton for ADCs, 2017
Instructor, Guangdong Ocean University

FDCT Projects

- High-performance wideband data conversion interfaces for an evolving informative world, 055/2012/A2, MOP4,332,630
- Design of digitally-controlled low-dropout regulators, 122/2014/A3, MOP1,174,300
- Development of a system-in-a-chip (SOC) integrated circuit for closed-loop neuronal manipulation of in vivo behaving animals , 093/2015/A3, MOP1,225,000
- Design of voltage references and regulators for IoT, 093/2016/A, MOP320,000
- Integration of Digital & Channel Microfluidic Systems for High-throughput Drug Screening, 110/2016/A3, MOP1,923,000
- R&D Timing Interleaving Techniques in Multi-channel High-speed Data Converters for Communication Systems, 117/2016/A3, MOP1,636,000
- Study and design of DC-DC KY boost converters in nanoscale CMOS technology, 120/2016/A3, MOP1,200,000
- Research on mm-size Extremely Power-Constrained Implantable ECG System on Chip Design, 006/2016/AFJ, MOP1,808,000, **NSFC-FDCT Joint Project**
- Low DC-link voltage and wide operation range hybrid grid-connected inverter for integrating renewable energy generation and power quality conditioning, 025/2017/A1, MOP1,110,000
- Research of Power Efficient Wideband Oversampling Delta-Sigma Modulator ADCs, 076/2017/A2, MOP1,247,200
- R&D Wideband Delta Sigma Modular for Next Generation LTE Mobile Communication Standard, 077/2017/A2, MOP1,540,000
- Research and Realization of Ultra-low-power Phase Quantizer and Power Management for IoT Wireless Communication Application, 0068/2018/A2, MOP1,543,000
- Low-Phase-Noise Wideband Oscillators and Frequency Synthesizers for 5G mm-Wave Transceivers in CMOS, 0044/2019/A1, MOP1,469,000
- Pico-pipette in Digital Microfluidic System for Precise Sample Delivery with Wide Range, 0053/2019/A1, MOP2,243,000
- Hybrid DC-DC Converter with High Efficiency High Power Density and Large Voltage Conversion Ratio, 0093/2019/A2, MOP1,777,000
- Research and Development of Ultra-low-power PUF circuits for emerging IoT Systems, 0108/2019/A2, MOP1,550,000
- Ultra Low Power Analog Edge Computing Artificial Intelligence Chip for Internet-of-Things, 0110/2019/A2, MOP1,266,800
- An integrated design for Real-time Closed Loop Optogenetic Neural Control (CLONC) system for advanced neuroscience applications, 0144/2019/A3, MOP1,182,000
- Research on Power Management System for Multi-core CPU, 0145/2019/A3, MOP1,605,000
- Research on Key Technologies of Millimeter Wave Sampling Ultra-High Speed Analog-to-Digital Converter, 0003/2019/AFJ, MOP1,953,500, **FDCT-MOST Joint Project**
- SeaSenseX - Next-generation microsensors for marine mutagens and carcinogens, 0011/2019/APJ, MOP1,000,000, **FDCT-FCT Joint Project**
- Digital Microfluidic Chip for Fast Coronavirus Detection (Anti-NCP epidemic), 0018/2020/A, MOP408,000, **Novel Coronavirus Pneumonia (NCP)**

PROJECTS

- Research on Key Control Technologies of Dynamic Wireless Power Transfer System for Electric Vehicles, 0028/2020/A1, MOP1,288,000
- Ultra-Low-Voltage (sub-0.5V) Single-Crystal-Multi-Clock Reference System for Energy-Harvesting IoT Devices, 0043/2020/A1, MOP1,360,000
- Customized high-voltage interfacing silicon-on-insulator integrated circuit for miniaturized magnetic resonance imaging system, 0071/2020/A2, MOP1,389,000
- Research and Development on Ultra-Compact Energy Harvesting Power Management IC for mm-Scale Internet of Things Application, 0148/2020/A3, MOP1,987,000
- Development and Industrialization of New Generation of Shipborne Solid-State Navigation Radar, 0036/2020/AGJ, MOP1,012,000, **FDCT-GDST Joint Project**
- Development and Industralization of Mobile Robotic Core Integrated Circuits Based on Simulataneous Localization and Mapping (SLAM) with Visual-LiDAR Fusion and Voice Interaction, 0052/2020/AGJ, MOP828,000, **FDCT-GDST Joint Project**
- Digital Microfluidic System for Breast Cancer Biomarker Detection and Drug Screening, 0072/2020/AGJ, MOP977,000, **FDCT-GDST Joint Project**
- Develop Power-Efficient High-Resolution GHz-Range Analog-to-Digital Converters in Advanced Nanometer-Scale Technology, 0004/2020/AKP, MOP11,957,000, **FDCT-AKP**
- R&D of Millimeter-Wave Multi-Resonant-Tank Voltage-Controlled Oscillator for 5G Communication, 0024/2021/A, MOP410,000

---

* **FDCT-NSFC**: The Science and Technology Development Fund - National Natural Science Foundation of China Joint Project

* **FDCT-MOST**: The Science and Technology Development Fund - Ministry of Science and Technology Joint Project

* **FDCT-FCT**: The Science and Technology Development Fund - Fundação para a Ciência e a Tecnologia (FCT) (Portugal) Joint Project

* **FDCT-GDST**: The Science and Technology Development Fund - Guangdong Department of Science and Technology Joint Project

* **FDCT-AKP**: FDCT Key Project

NSFC Fund

用於GPU的細粒度、全集成電源管理系統, 61974046, RMB590,000

用於毫米波無綫通訊應用的高能效模數轉換器, 61604180, RMB190,000

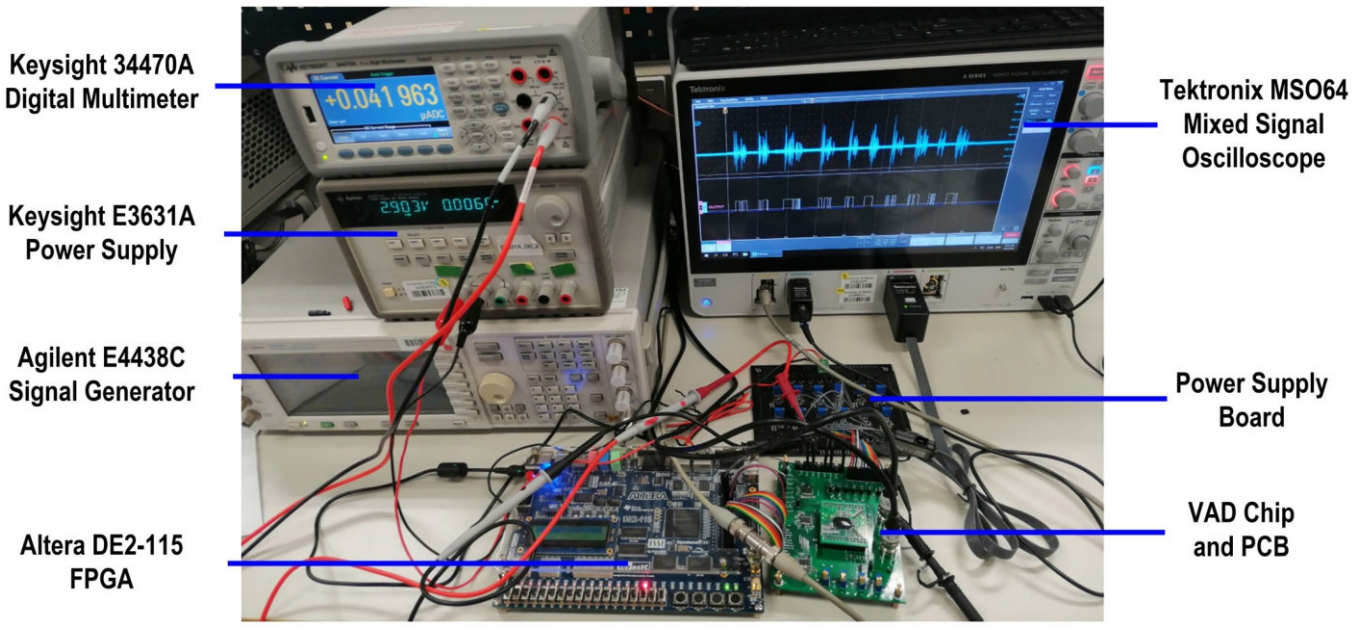
面向48V電源系統的高集成、低損耗混合結構負載點轉換器, 62104269, RMB240,000

Industrial Consultancy Projects

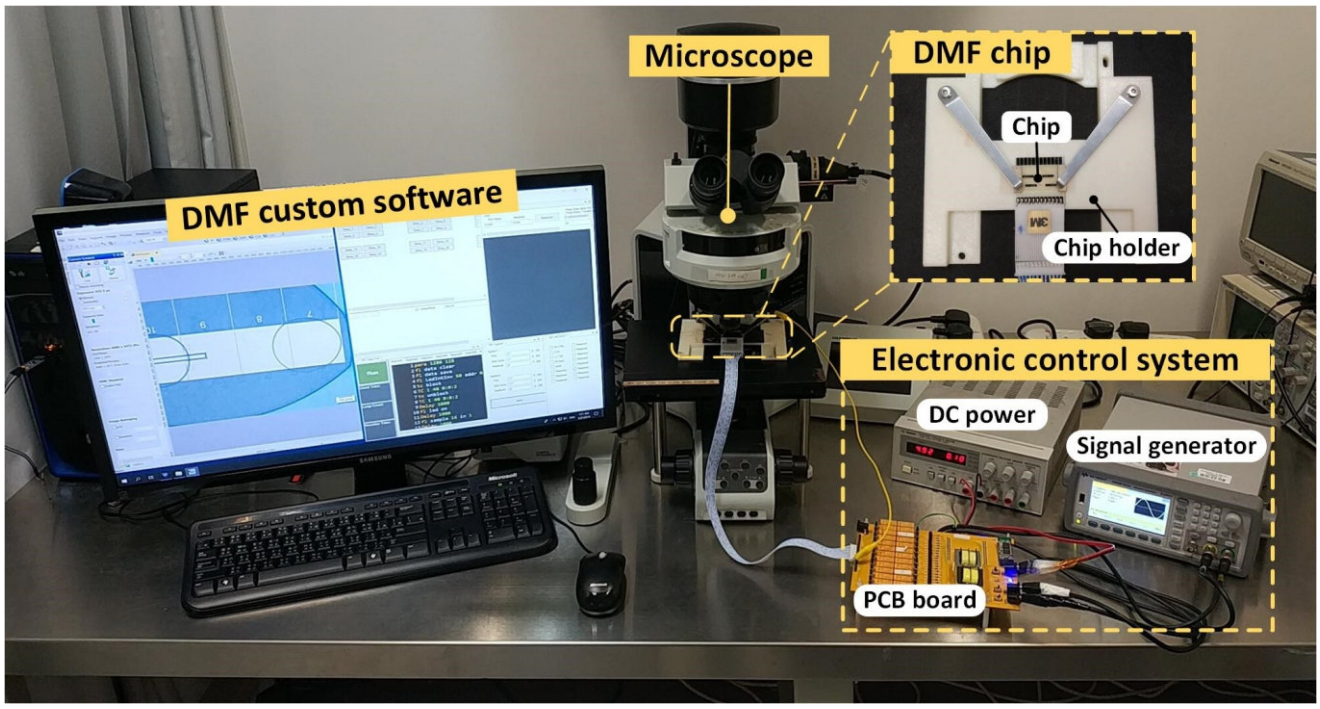
Over MOP 14,000,000 of industrial consultancy projects with companies in the Greater Bay Area, in the area of ADC, PLL, DC-DC Converter and microfluidics in 2017 – 2020.

EXPERIMENTAL PROTOTYPES

Experimental Setup of analog Voice Activity Detector (VAD).

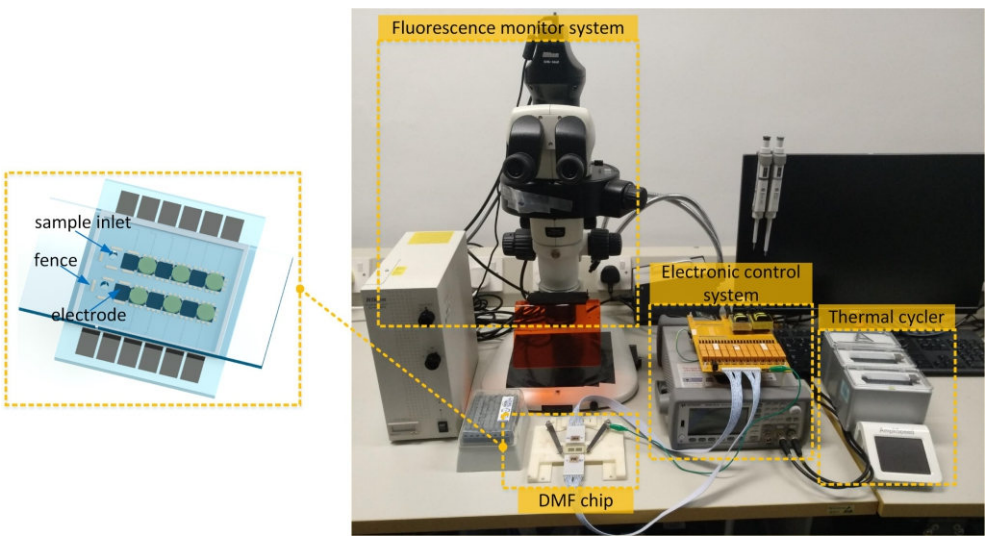


Satellite droplet ejection for sample delivery on DMF chip

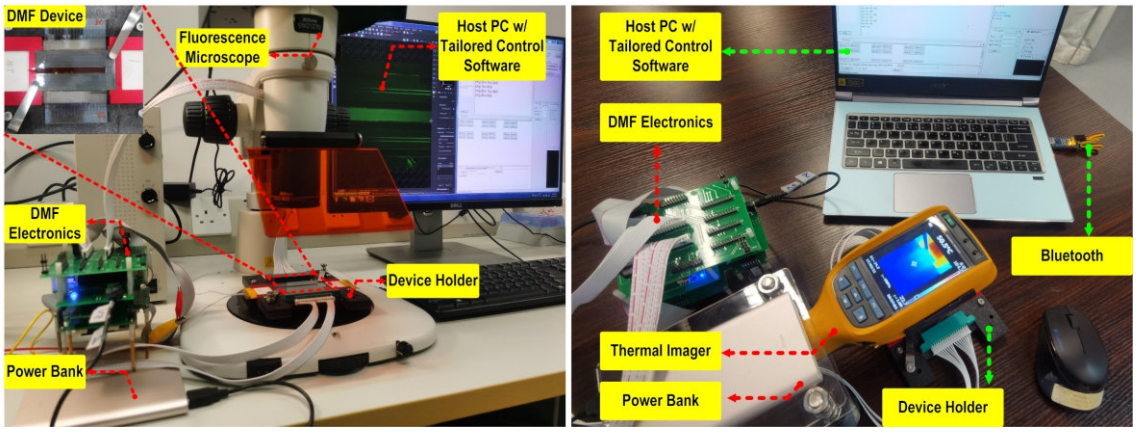


EXPERIMENTAL PROTOTYPES

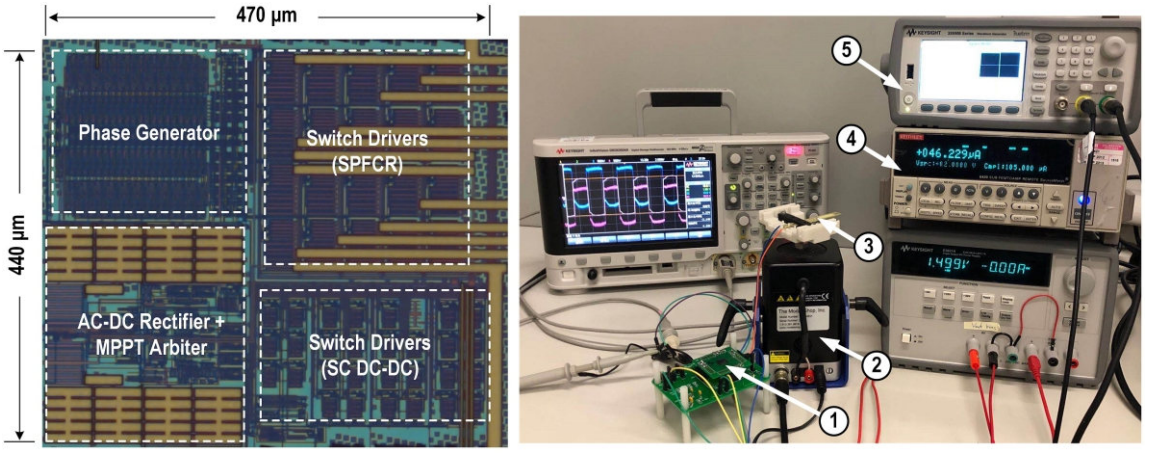
Clip to Release on Amplification (CRoA) for enhanced PCR on DMF



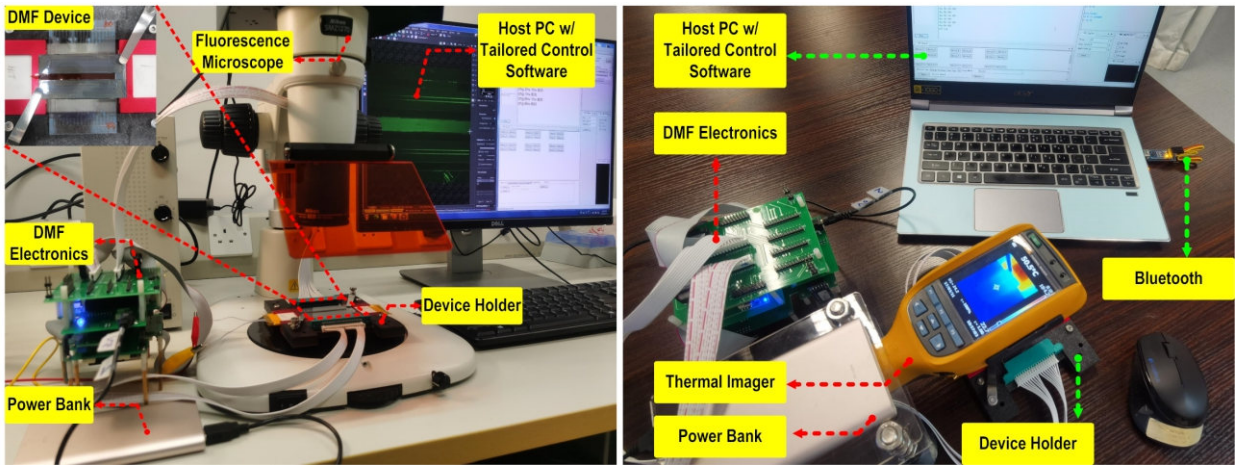
Experimental Setup for high-resolution MCA on DMF



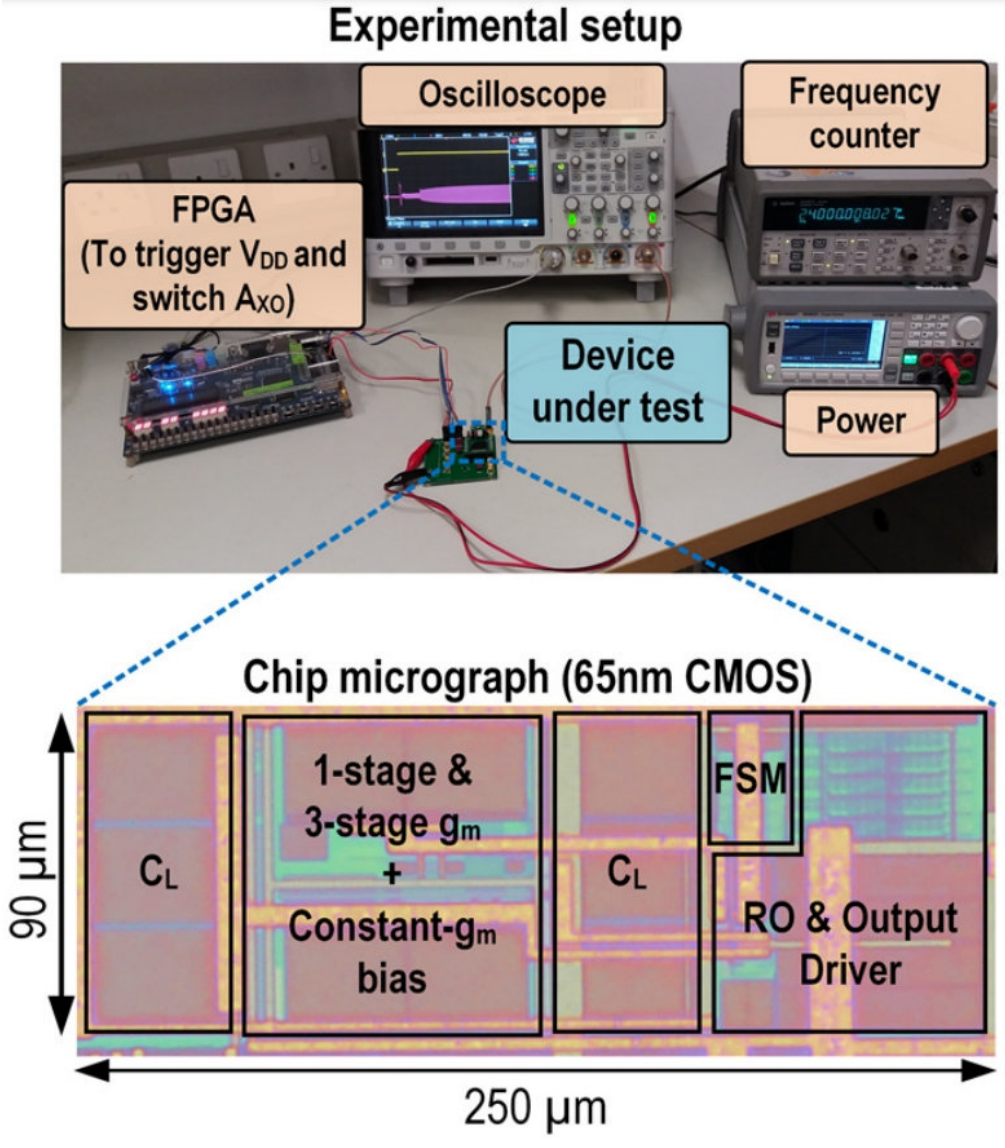
Chip micrograph and experimental setup for piezoelectric energy harvesting using SPFCR



Experimental setup for high-resolution MCA on DMF

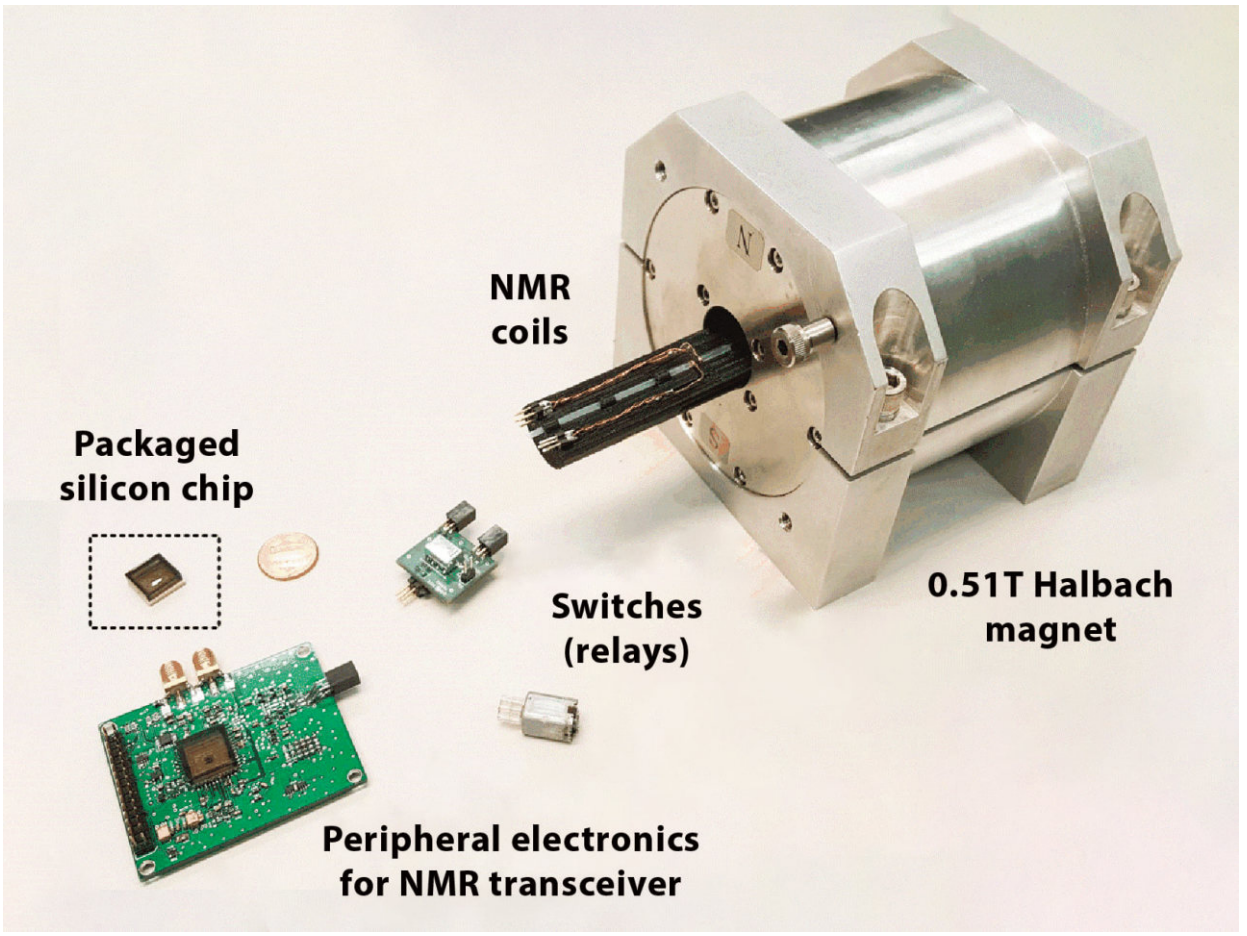


Experimental setup and die micrograph of the proposed fast startup crystal oscillator in 65nm CMOS

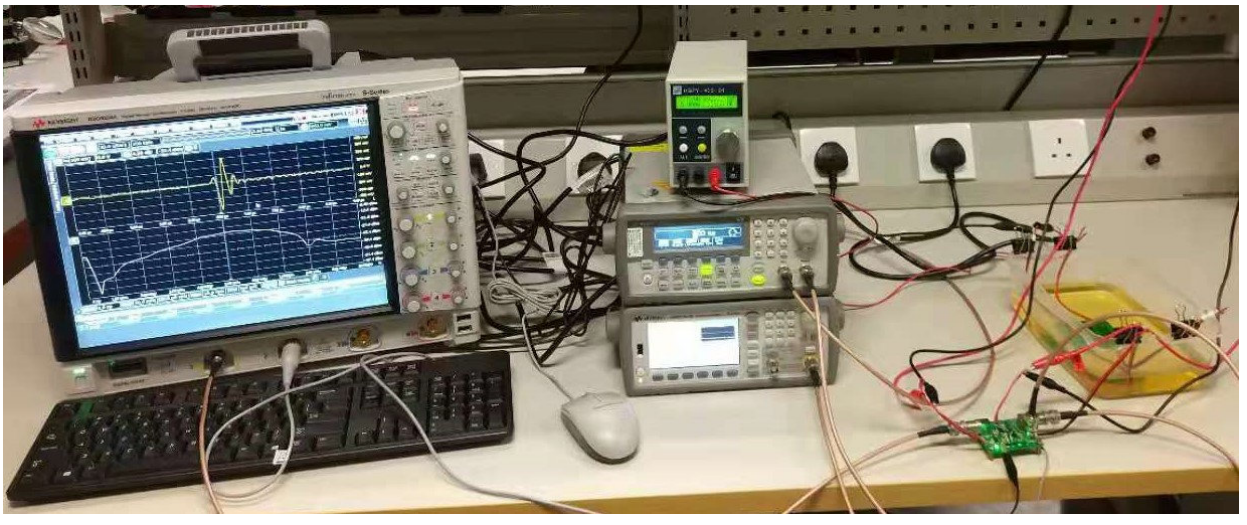


EXPERIMENTAL PROTOTYPES

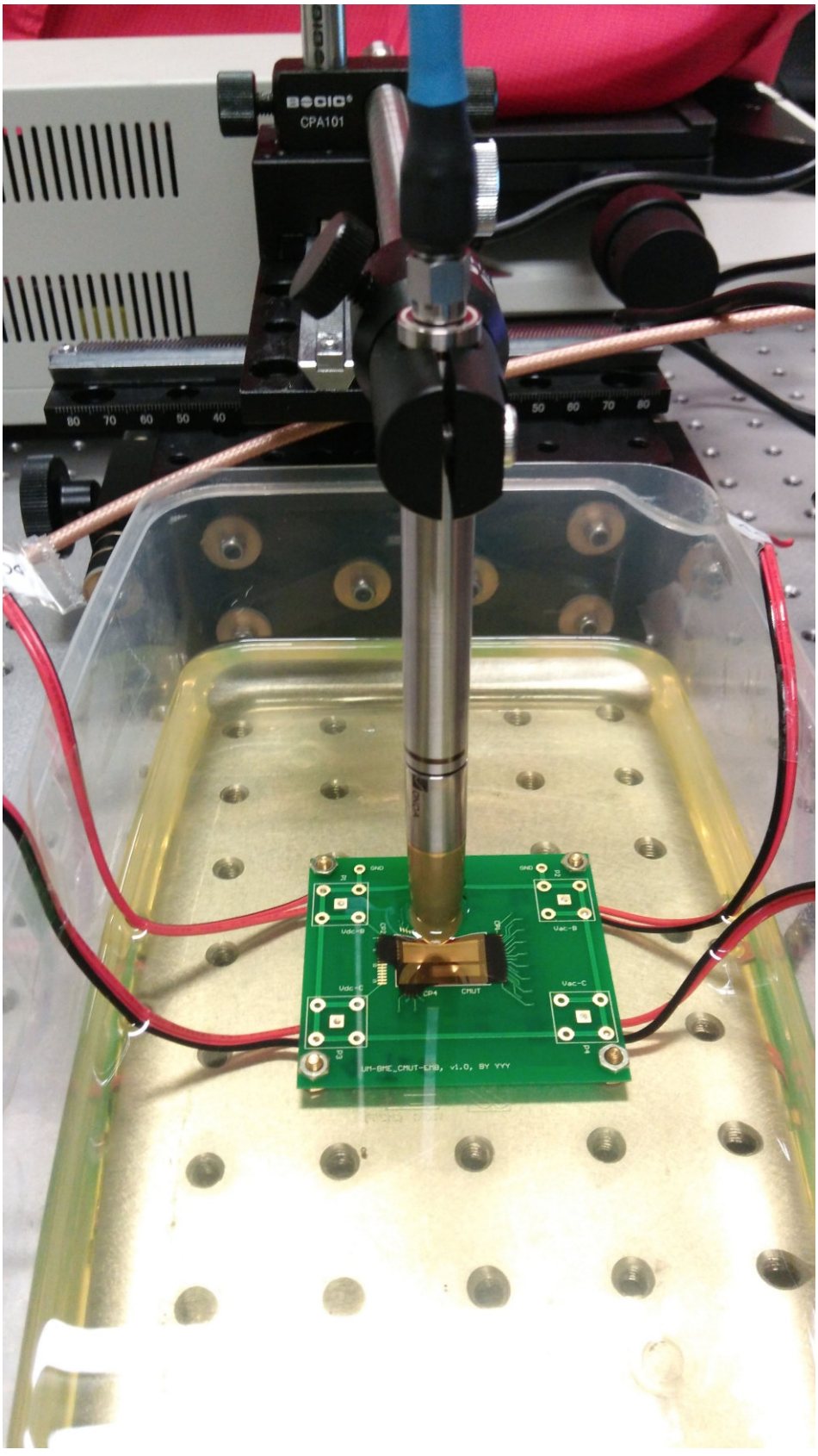
The hardware for the portable NMR platform with parallelism. The core of the platform is the CMOS NMR transceiver, which was packaged onto a chip carrier for testing.



Experimental setup for testing the multi-band CMUT

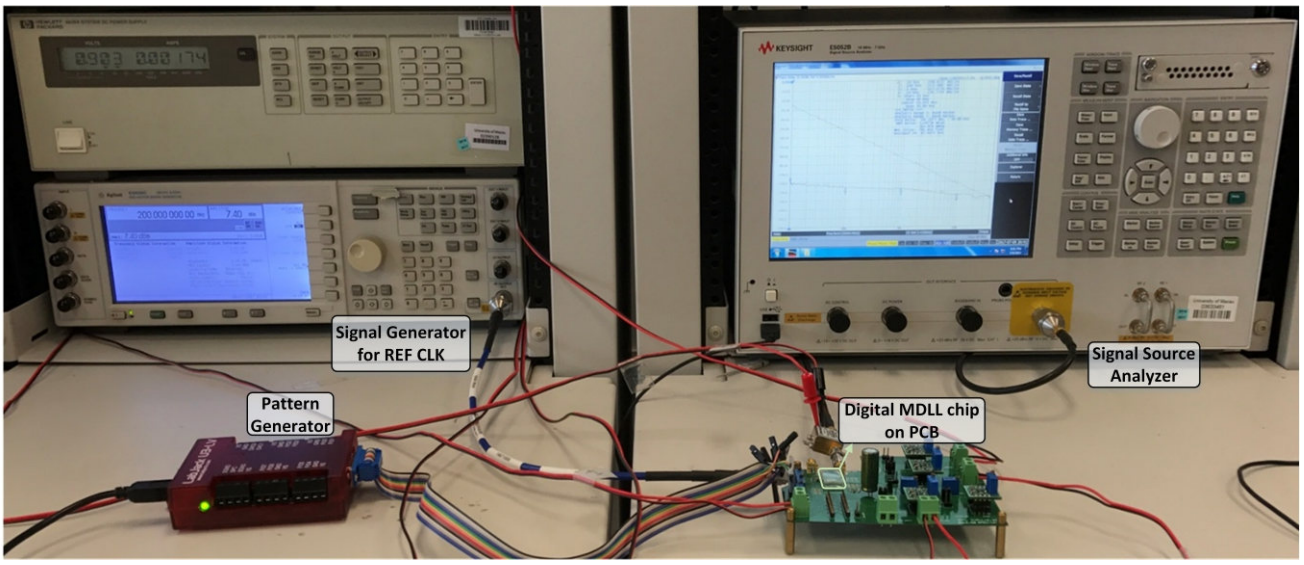


The acoustic performance measurement of the CMUT

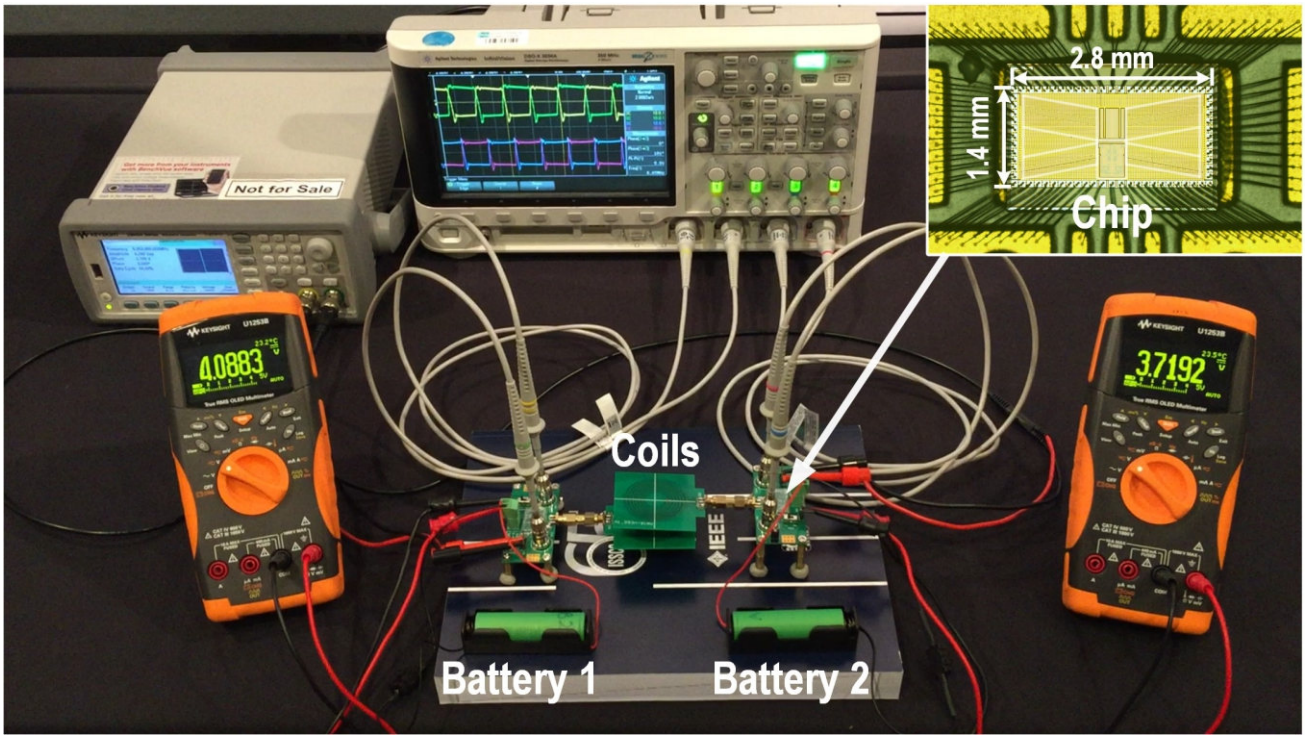


EXPERIMENTAL PROTOTYPES

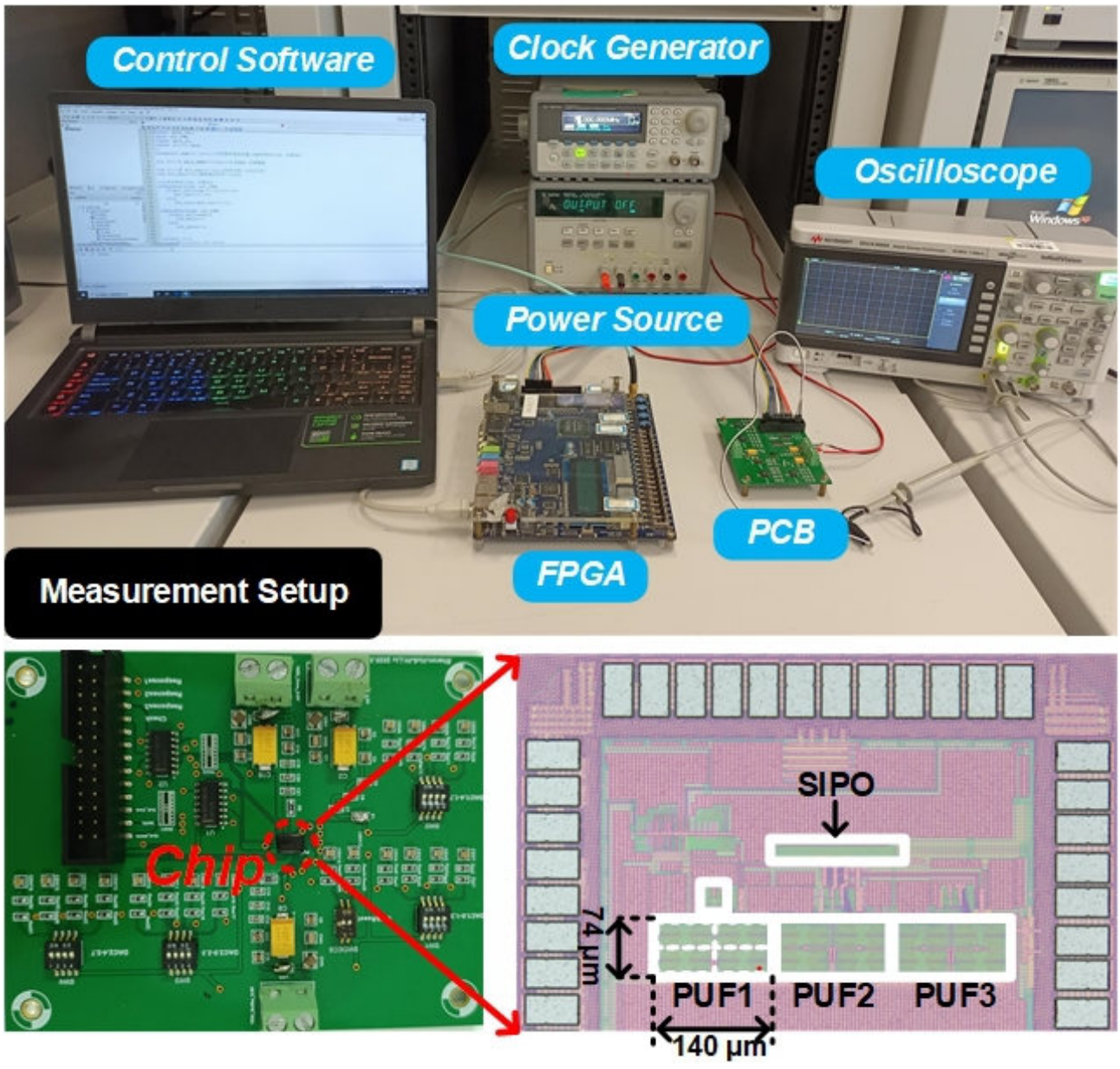
Measurement setup of a low-jitter digital Multiplying Delay-Locked Loop (MDLL)



Device-to-Device Bidirectional Wireless Power Transfer

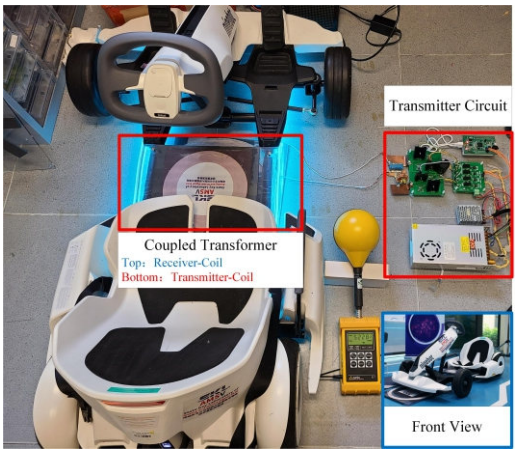


Experimental setup of strong physical unclonable function, PCB design and chip photo

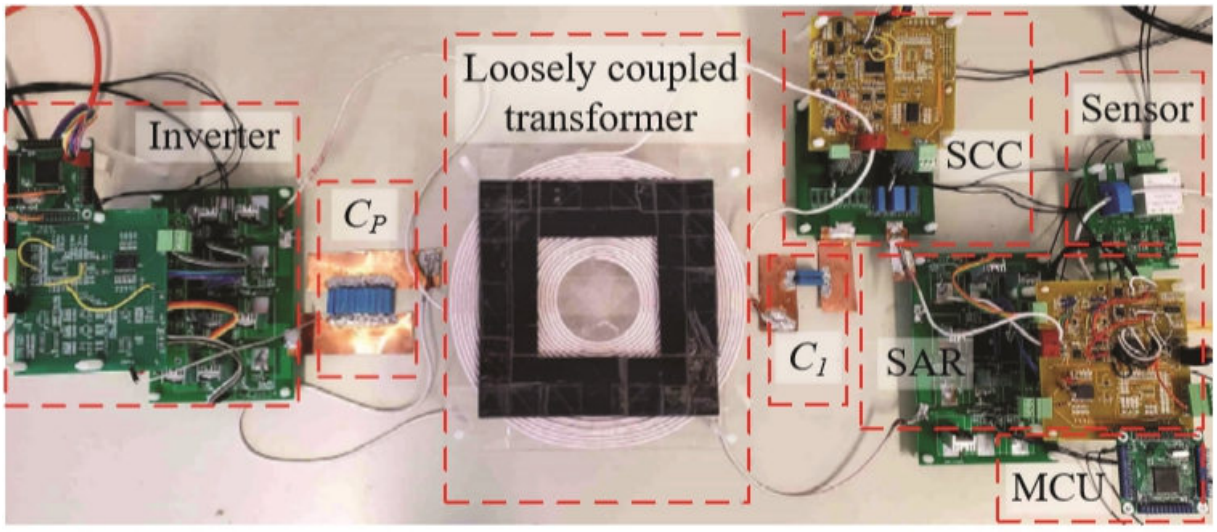


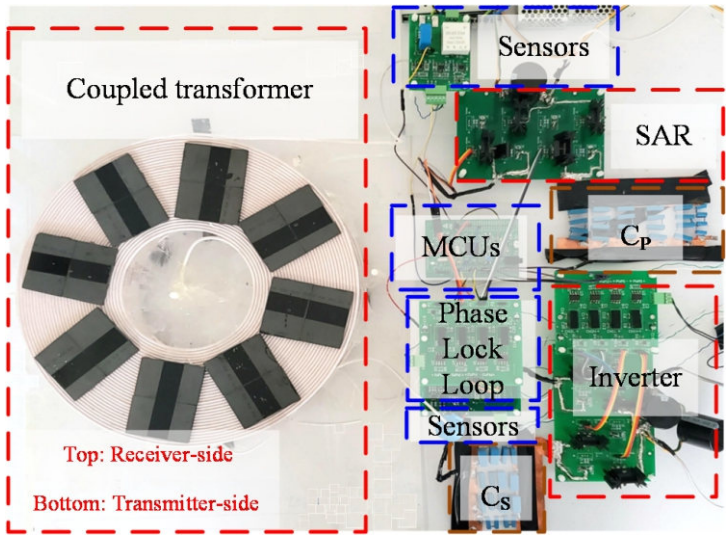
EXPERIMENTAL PROTOTYPES

A High-Misalignment-Tolerance Inductive Power Transfer Charger Experimental Prototype for Mini-EV



A Single-Stage Constant-Power Inductive Power Transfer Converter Experimental Prototype

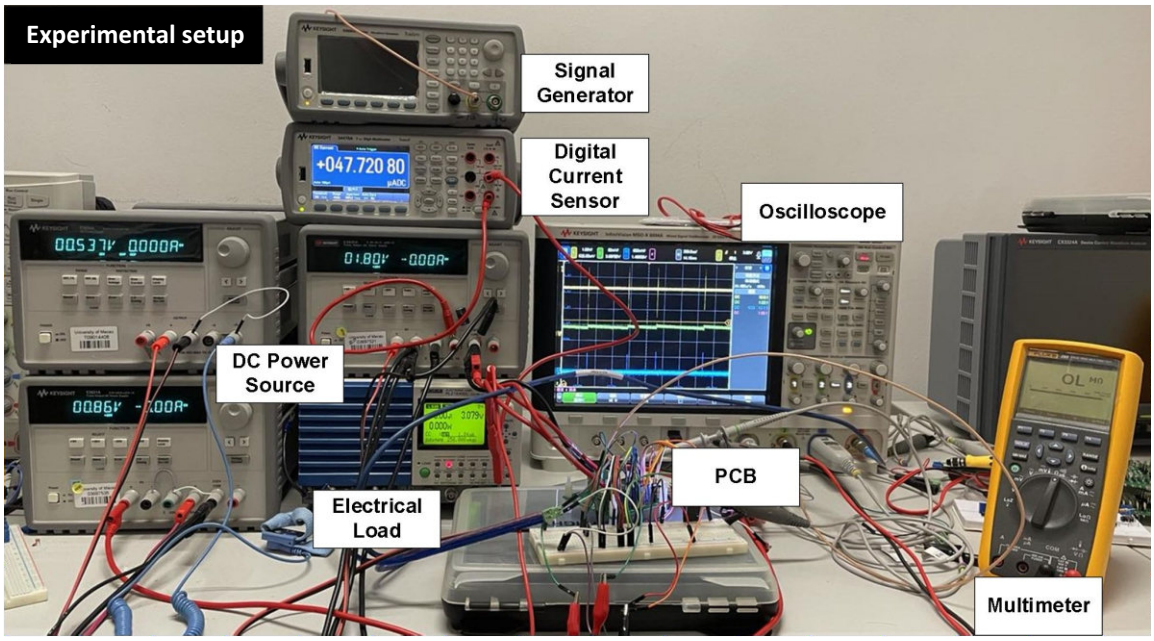




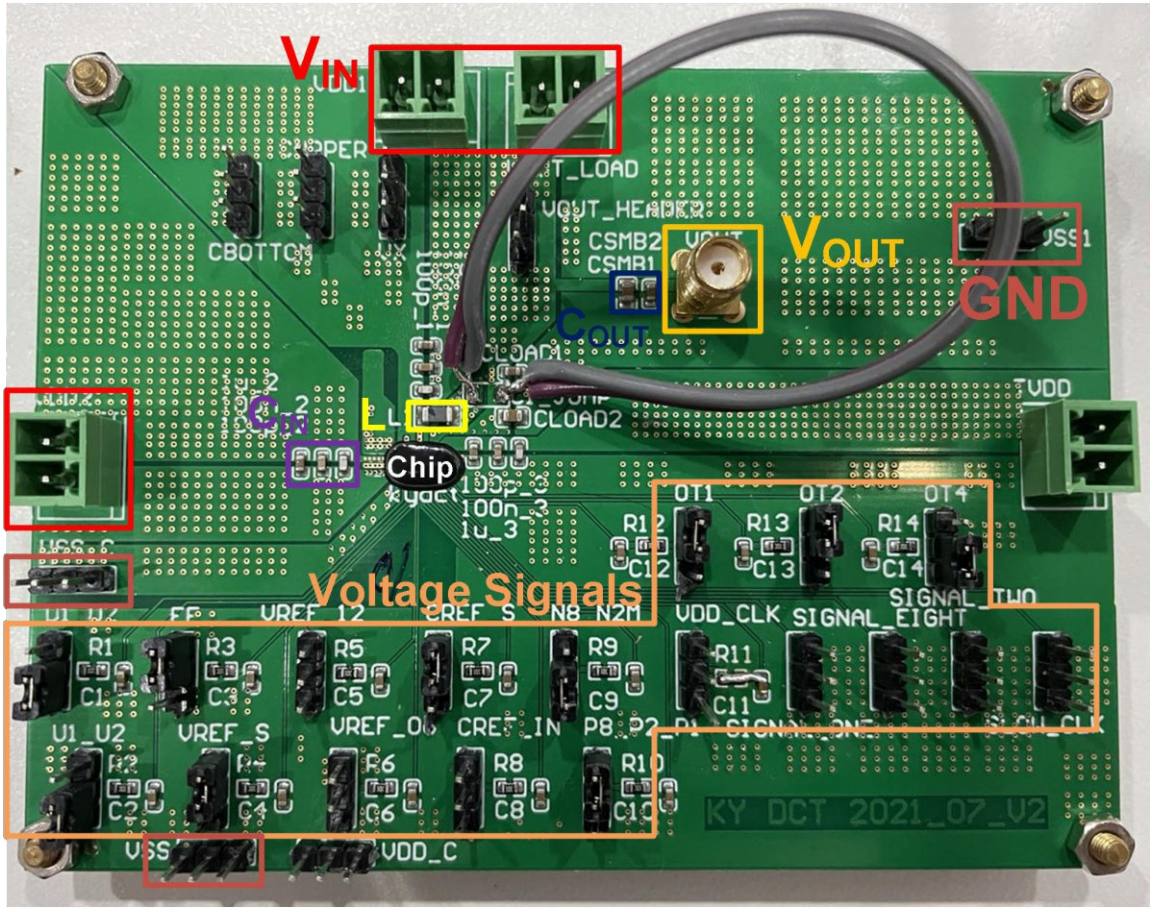
A Constant-Frequency and Non-Communication-Based Inductive Power Transfer Converter Experimental Prototype for Battery Charging

EXPERIMENTAL PROTOTYPES

Experimental setup of an ultra low quiescent current DC-DC converter system.

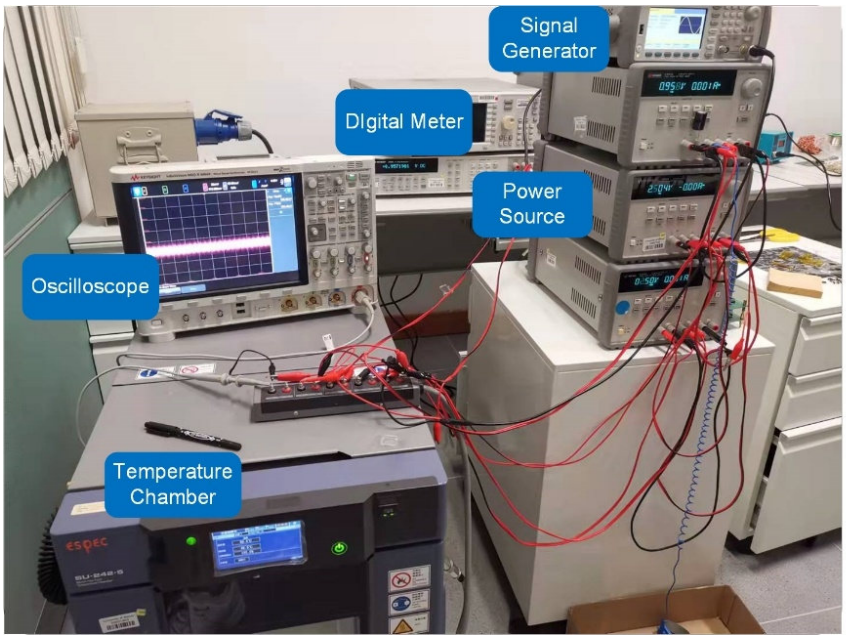


Prototype test board for an ultra low quiescent current DC-DC converter.

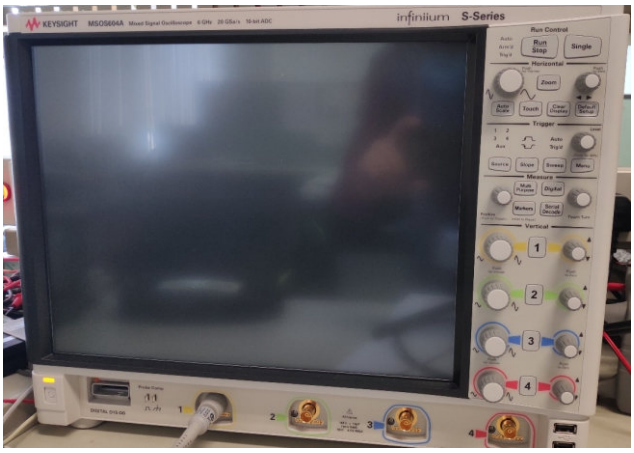


EXPERIMENTAL PROTOTYPES

Experimental setup for measuring the Bandgap Reference.



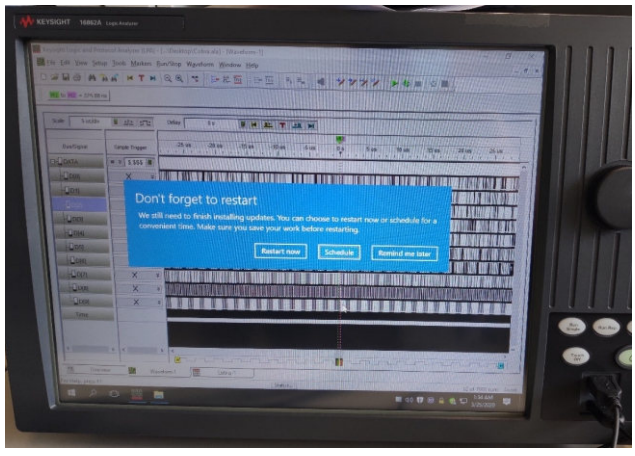
TESTING EQUIPMENT AND FACILITIES



Model: Keysight MSOS604A Mixed Signal Oscilloscope 6 Ghz

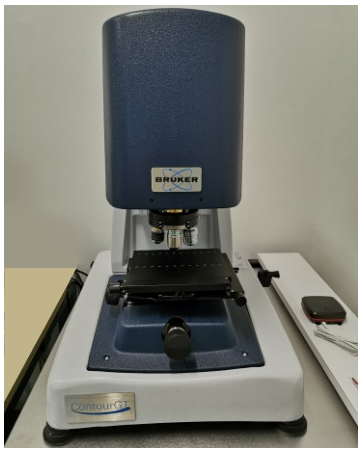
Model: Keysight DSAV334A Digital Signal Analyzer 33 Ghz

Model: Keysight PSG Analog Signal Generator E8257D 250kHz-20GHz



Model: Keysight 16862A Logic Analyzer

Model: U4164A Logic Analyzer



Model: Bruker Optical Profiler, GTK-M

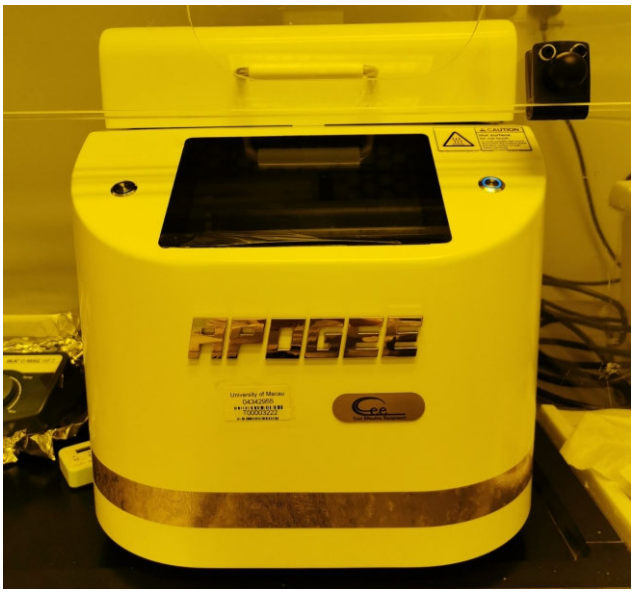
TESTING EQUIPMENT AND FACILITIES

Model: Thermo Scientific Dionex Ultimate 3000

Model: Nikon Motorized Inverted Microscope Ti2

Model: O2 Plasma Cleaner

Model: Mini DC Sputter System



Model: Apogee Hotplate System

TESTING EQUIPMENT AND FACILITIES

Model: California Instruments 3091LD Programmable Power

Model: YOKOGAWA DL850EV ScopeCorder

Model: Rack Server ProLiant DL380 Gen10

Model: Keysight U4164A Logic Analyzer

Model: Keysight Signal Source Analyzer E5052B 10 MHz – 7 Ghz

Model: Keysight MSOV204A Mixed Signal Oscilloscope 20 Ghz

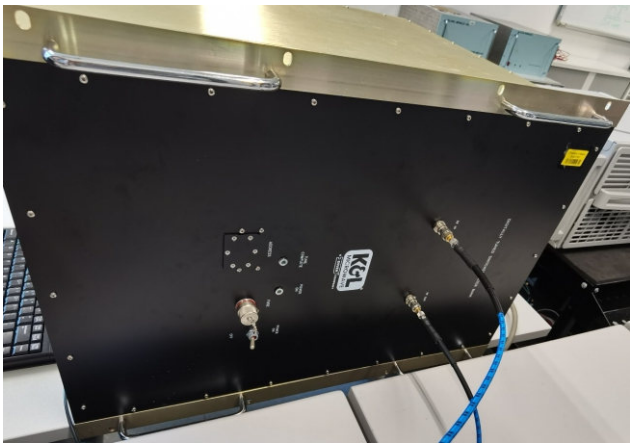
Model: Keysight MSOS804A Digital Storage Oscilloscope 8 Ghz

TESTING EQUIPMENT AND FACILITIES

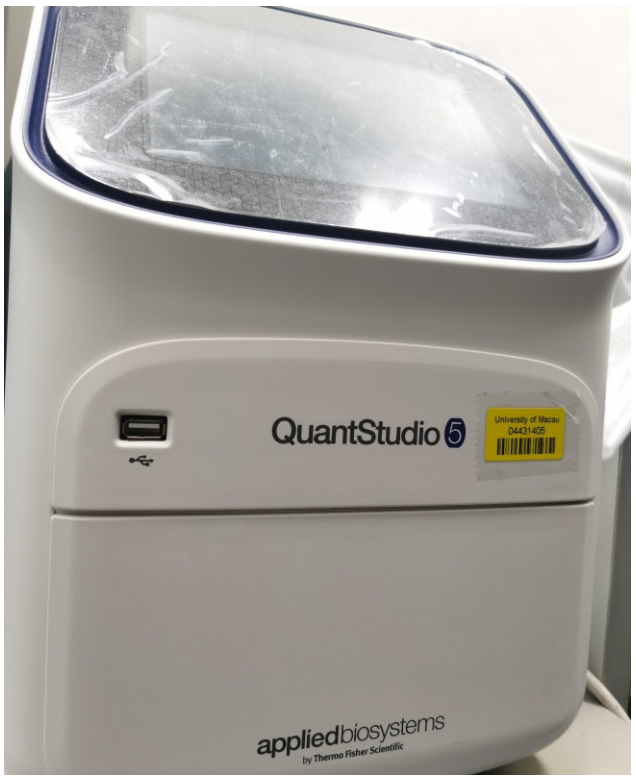
Model: Keysight MSOS404A Mixed Signal Oscilloscope 4 Ghz

Model: Keysight N6705C DC Power Analyzer

Model: K&L 4 MHz to 750 MHz Programmable Filter Module



Model: K&L 15 MHz to 4GHz Programmable Filter Module



Model: QuantStudio™ 5 Real-Time PCR System

Model: SeqStudio™ Genetic Analyzer System

TESTING EQUIPMENT AND FACILITIES

Model: Tresky T-3000-Pro Die Bonder & Component Placer

Model: Fujifilm Dimatix Materials Printer DMP-2850

Model: Profilm 3D Optical Profiler

TESTING EQUIPMENT AND FACILITIES

CAD Design Class Laboratory

TESTING EQUIPMENT AND FACILITIES

Chip Fabrication and Measurement Laboratory

TESTING EQUIPMENT AND FACILITIES

PCR and Equipment Room

TESTING EQUIPMENT AND FACILITIES

Server Room

CORE SWITCH

H3C 10508 x 2: Switching capacity 106.2Tbps

STORAGE CAPACITY

EMC Isilon S210: 3 nodes, 39TB raw and 60Gbps parallel data connections
EMC Isilon X210: 4 nodes, 176TB raw and 80Gbps parallel data connections
EMC Isilon F800: 4 nodes, 96TB raw and 320Gbps parallel data connections
EMC Isilon H500: 4 nodes, 240TB raw and 320Gbps parallel data connections
EMC Isilon A200: 4 nodes, 480TB raw and 80Gbps parallel data connections

CLOUD COMPUTING SERVERS

Over 100 Servers and 300 PC clients, 2376 CPU cores and 11TB RAM in total.
Can run 256 multi-core microelectronics simulations simultaneously.

SOFTWARE AND EDA TOOLS

- Cadence: Custom Integrated Circuits Bundle (140 licenses), Digital Integrated Circuits Bundle (20 licenses)
- Mentor Graphics: Nanometer design bundle (30 licenses)
- Synopsys: Front-end University Bundle (7 licenses)
- Sonnet Professional with Floating Network License with High-Performance Solver Engine
- Matlab and Simulink
- OpenText OpenText Exceed TurboX

澳門大學
UNIVERSIDADE DE MACAU
UNIVERSITY OF MACAU

模擬與混合信號超大規模集成電路
國家重點實驗室
Laboratório de Referência do Estado em
Circuitos Integrados em Muito Larga Escala
Analógicos e Mistos
State Key Laboratory of
Analog and Mixed-Signal VLSI

微電子研究院
Instituto de Microelectrónica
Institute of Microelectronics